SOLUTIONS BEYOND LIMITS

IPC Northwest Design Council

July 26, 2012

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Micro BGA Design Guidelines

- 0.8 mm pitch (when microvias should be considered)
- 0.5 mm
- 0.4 mm
- 0.3 mm
- 0.25 mm

Engineering Considerations For Via Structures

Standard through hole technology:
Channel density limited by via density, geometry and pitch

Microvias:
Channel density enhanced through smaller geometry
Limited Z axis connectivity

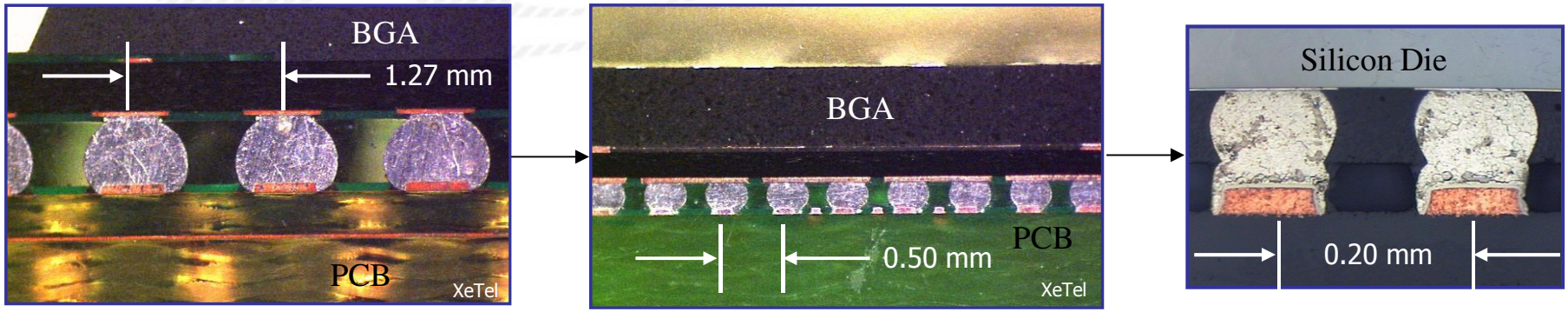
Blind & Buried via's:
Channel density enhanced
Still geometry limited
Limited Z axis connectivity

SMV:
Channel density enhanced through smaller geometry
Unlimited Z axis connectivity

Once you leave through hole designs the goal is to find the via combination that maximizes routing channel density at the lowest cost

Density Trends In Array Packages

Increasing I/O Density → Chip Scale Packaging → Flip Chip Packaging



1.27 mm BGA package
Localized via density
62/cm² (400/in.²)

6.45 x Increase
in via density

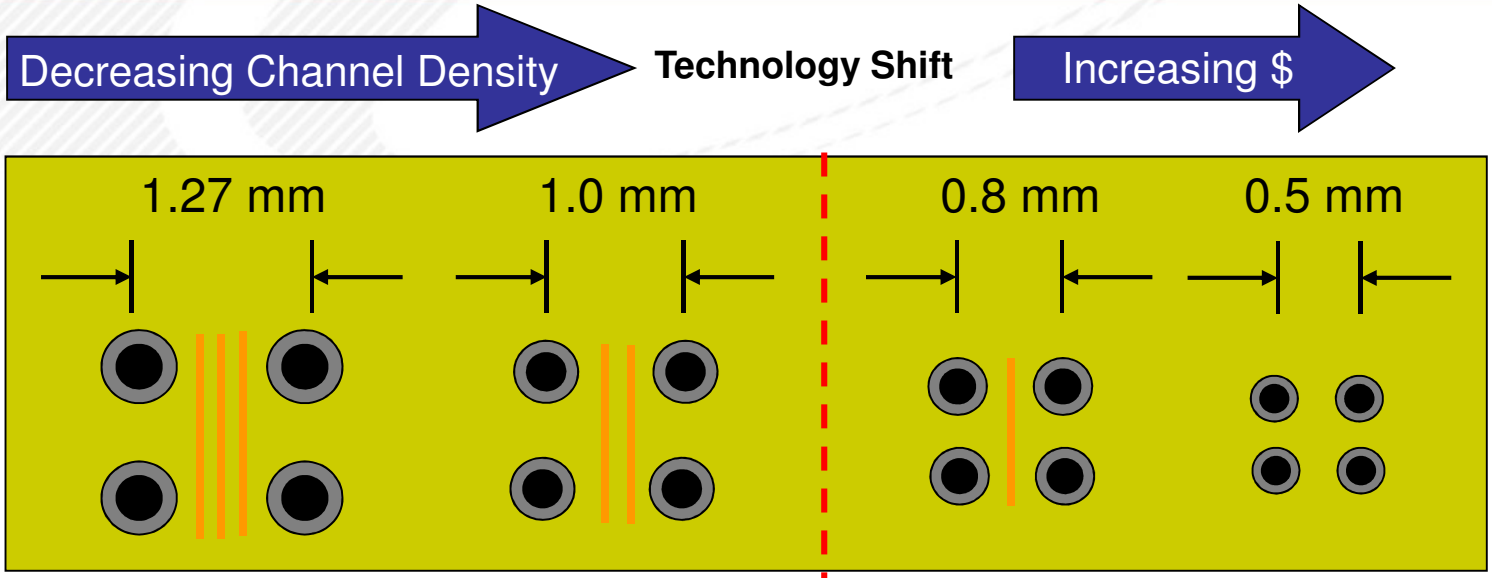
0.50 mm BGA package
Localized via density
400/cm² (2580/in.²)

6.25 x Increase
in via density

0.20 mm Flip Chip
Localized via density
2500/cm² (16,129/in.²)

Circuit Density & Mechanical Drilling limitations

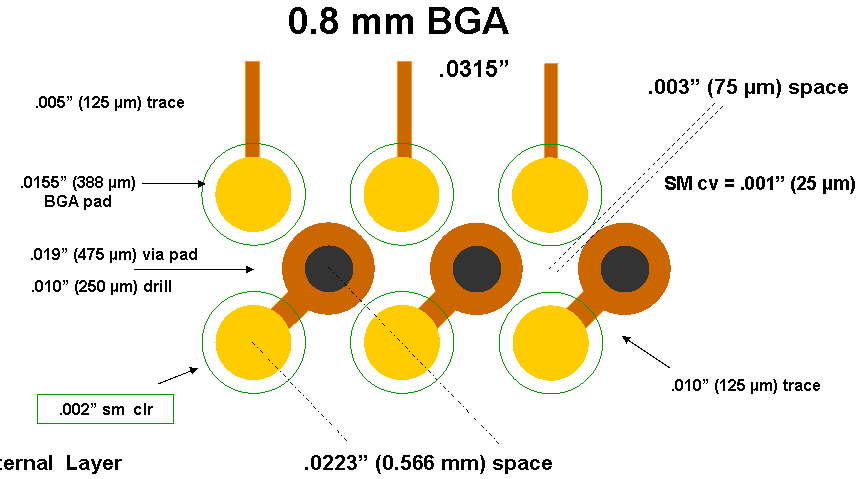
Circuit Density vs BGA Pitch (Mechanical Drill)



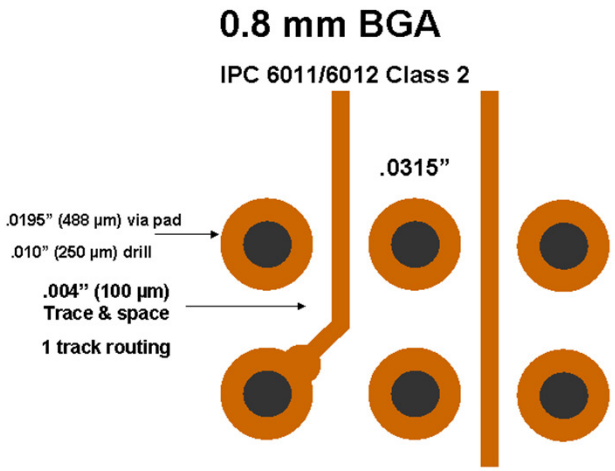
Drill dia.	0.010” (250 µm)	0.010” (250 µm)	0.008” (200 µm)	
Pad dia.	0.022” (550 µm)	0.019” (475 µm)	0.018” (450 µm)	0.010” (250 µm)
Line width	0.004” (100 µm)	0.004” (100 µm)	0.0045” (112 µm)	N/A
Space	0.004” (100 µm)	0.004” (100 µm)	0.0045” (112 µm)	
				Escape Only !
Thickness	Up to 0.100”	Up to 0.100”	Up to 0.062”	

Microvias add Value at 0.8 mm pitch

0.8 mm BGA
Design Guidelines
IPC 6011 / 6012
Class 2



Thickness of .093" (2.362 mm) - .100" (2.54 mm) Aspect Ratio 10:1



Thickness of .093" (2.362 mm) - .100" (2.54 mm) Aspect Ratio 10:1

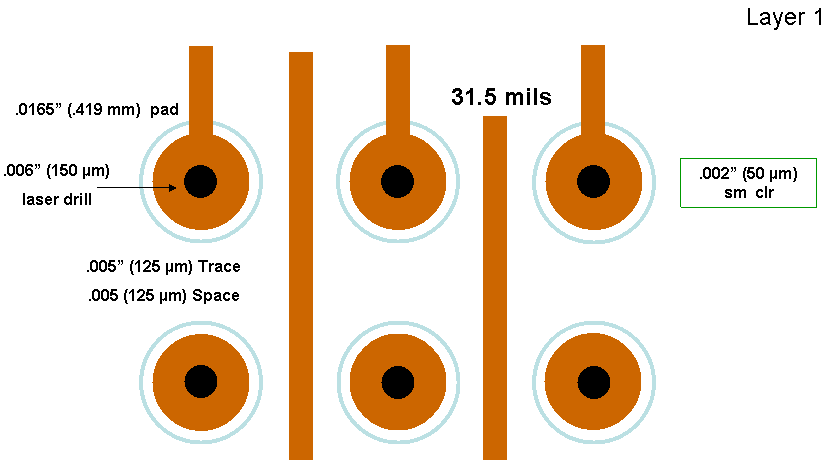
Thickness of .093" (2.362 mm) - .100" (2.54 mm) Aspect Ratio 10:1

Microvias add Value at 0.8 mm pitch

0.8 mm BGA

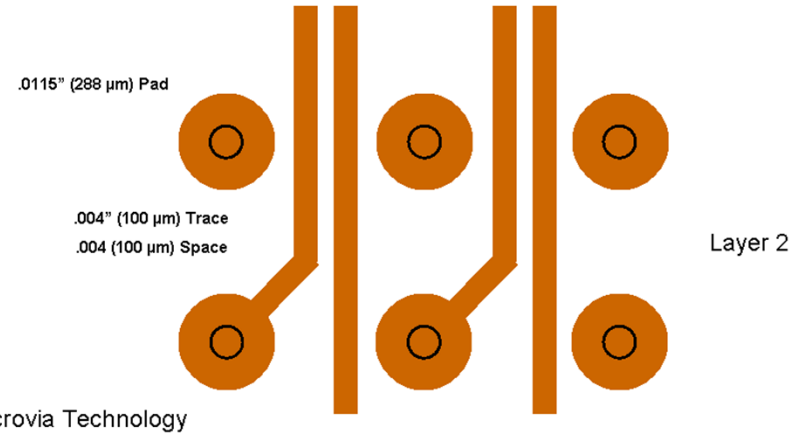
Microvia Technology

0.8 mm BGA Design



Microvia Via-in-Pad Technology = Eliminates through vias

0.8 mm BGA Design



0.8 mm BGA Design

No clearance required

Laser Drilling Technology & Microvias

What is considered a Microvia ?

- Laser Drilled Blind Via from the outer layer to an inner layer
- 150 µm (0.006”) diameter laser drill (range 100 µm (0.004”) – 200 µm (0.008”)
- Laser drill directly into BGA or SMT footprint (Via-in-Pad)
- Eliminate through-hole vias
- Increases routing density & enhance electrical characteristics
- Maintain 0.5:1 aspect ratio or advanced 0.8:1
- Provides fan-out solutions
- Laser microvia’s terminate to the underlying pad without penetrating the copper

Microvia Types

- Standard – Single Lamination cycle (no Buried Via)
- Standard – with buried via
- Staggered or stair-step
- Off-set Microvias
- **Stacked MicroVias are required for 0.4 mm pitch and below**
- Deep Microvias

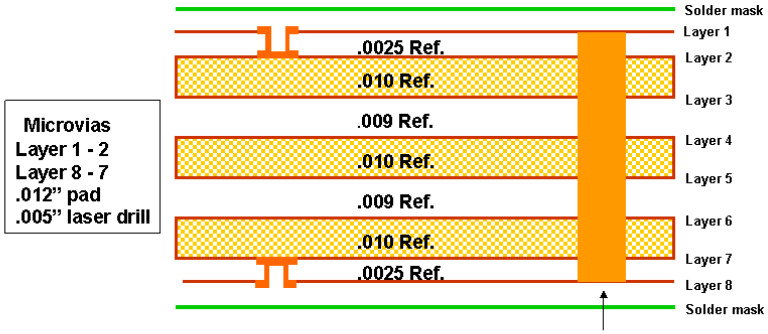
Microvia Generations

- **Standard Microvias** create routing density (eliminate through vias)
  - Reduce layer count
  - Enhance electrical characteristics
  - Standard Microvias limited to layers 1 – 2 & 1 - 3
- **Stacked Microvias (SMV™)** allows increased routing on multiple layers
  - Provide Solutions for next generation applications
  - 1 mm – 0.8 mm – 0.65 mm - 0.5 mm – 0.4 mm – 0.3 mm & 0.25 mm
  - SMV provides solid copper plate, eliminating potential solder voiding
- **Deep Microvias (DpMV™)** provide additional dielectric material & small geometry features, improved Impedance performance & provides RF microvia solutions
- **Deep Stacked MicroVias (DpSMV™)**

  Provides additional dielectric while maintaining small geometries on multiple layers

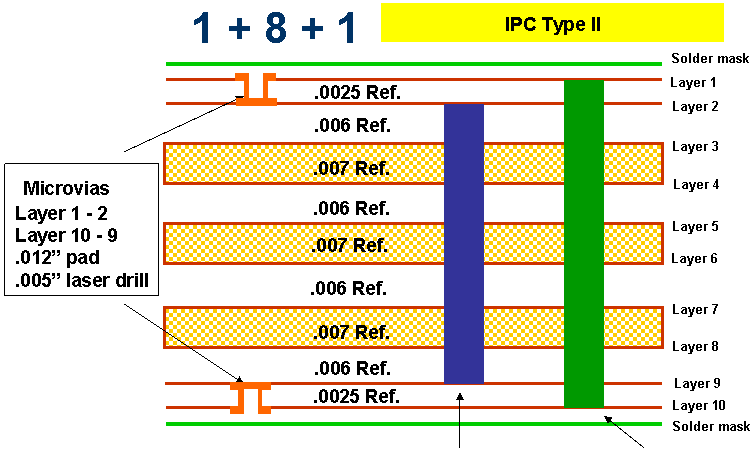
Microvia Types

1 + 6 + 1 — IPC Type I



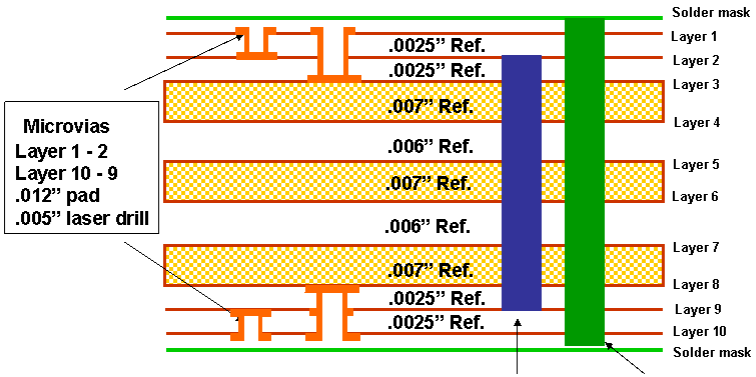
Finish Thickness = .062 +/- .006
Material = High Temp FR4

1 + 8 + 1 — IPC Type II



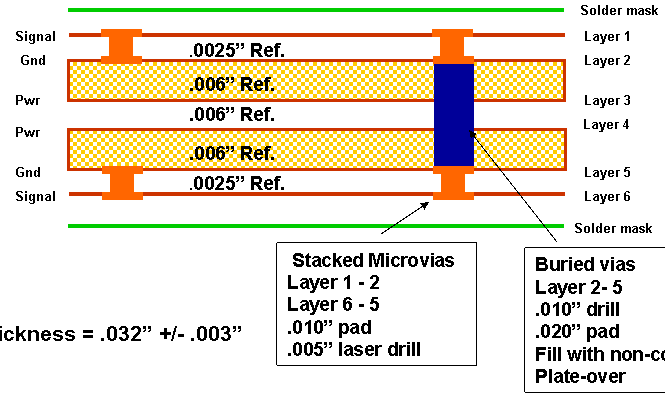
Finish Thickness = .062" +/- .006"
Material = High Temp FR4

2 + 6 + 2 — IPC Type II – Variable depth



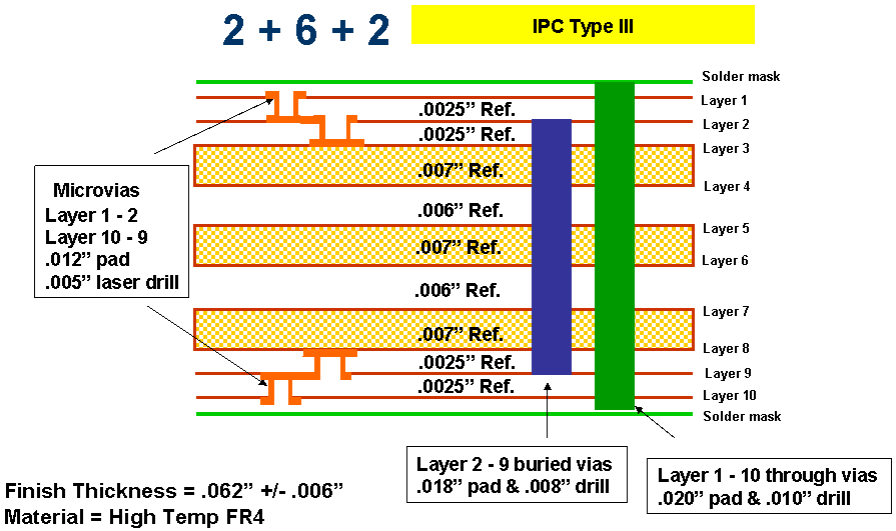
Finish Thickness = .062" +/- .006"
Material = High Temp FR4

1 + 4 + 1 — IPC Type II – stacked vias

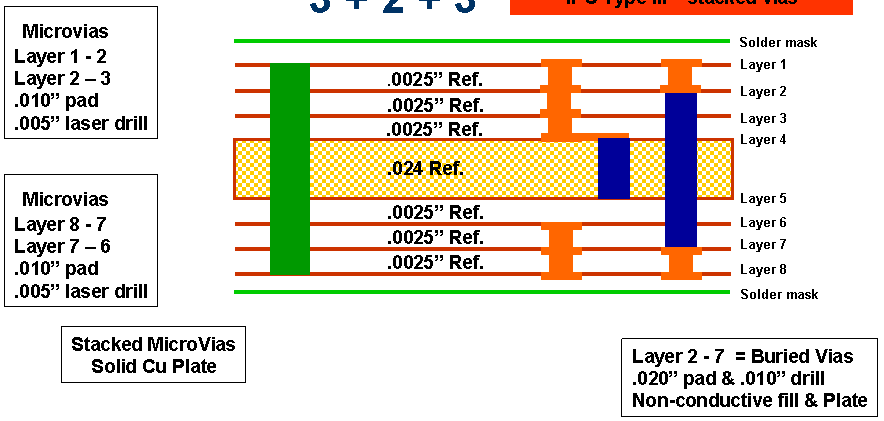


Finish Thickness = .032" +/- .003"

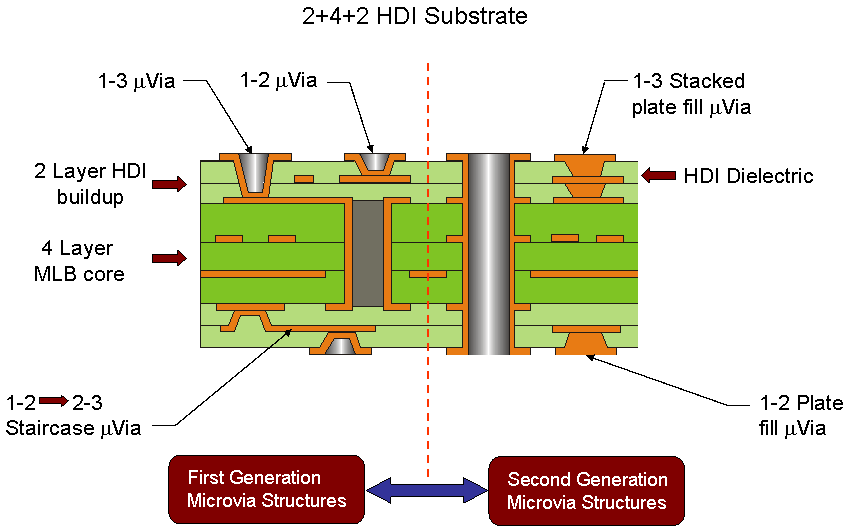
Microvia Types



Finish Thickness = .062" +/- .006"
Material = High Temp FR4



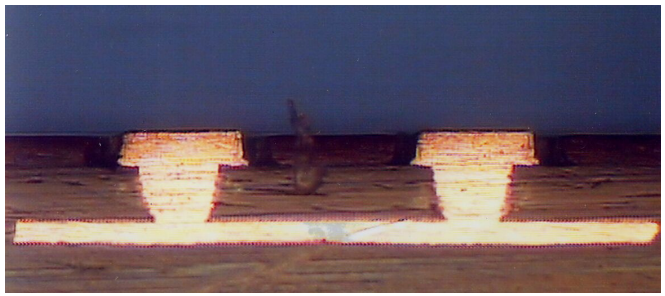
Finish Thickness = .048 +/- .004
Material = High Temperature FR4



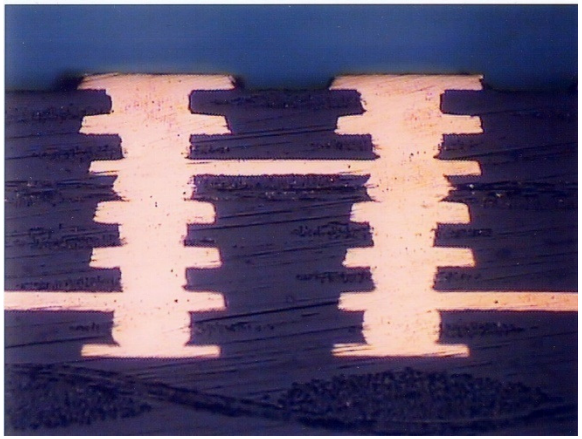
Second Generation Microvias

Definition:

0.005” (125 µm) laser drilled MicroVia



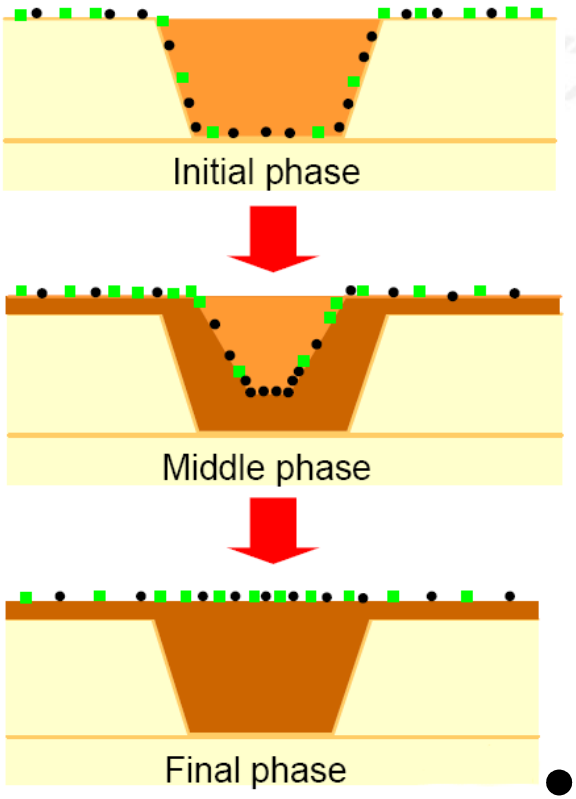
Single - SMV™ Technology



Stacked MicroVias (SMV™)

Stacked MicroVia (SMV®) Technology

Electroplated Copper via filling Mechanism



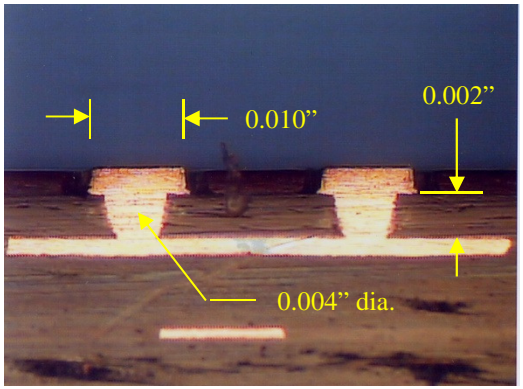
- Bottom-up filling behavior is attributed to the action of organic additives(must be controlled to prescribed limits)
- Suppressor rapidly forms current inhibiting film on Cu surface. Film has little geometric dependence due to high suppressor solution concentration
- Accelerated bottom-up fill behavior is due to a local accumulation of brightener species at the feature base
- As surface area is reduced during deposition, the concentration of brightener species increases, resulting in a non-equilibrium surface concentration. This local concentration of brightener accelerates the plating rate relative to the surface.

● Brightener

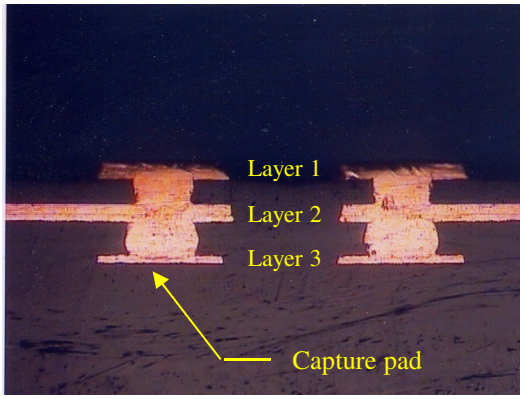
■ Carrier

Source: ROHM AND HAAS ELECTRONIC MATERIALS CIRCUIT BOARD TECHNOLOGIES

Planar Microvia



Stacked Microvia



Stacked MicroVia (SMV®) Technology

Advantages:

- **Design flexibility (SMV post or buried SMV) single or stacked**
- **Provides a solid copper plate**
- **Improves Current Carrying Capability & Thermal Management**
- **Provides a Planar surface for BGA (Via-in-Pad)**
- **Increases routing density for Fine Pitch BGAs**

  (0.65 mm, 0.5 mm, 0.4 mm, 0.3 mm & 0.25 mm)
- **Allows Design Fan-out on multiple layers using 0.010" (250 µm), 0.008" (200 µm), and 0.007" (175 µm) pad diameters**

Stacked MicroVia (SMV®) Technology

Design Guidelines:

- ***Standard***
  - **0.010” (250 µm) Pad diameter & 0.005” (125 µm) laser drill**
- ***Advanced***
  - **0.0086” (218 µm) Pad diameter & 0.005” (125 µm) laser drill**
- ***Flip Chip Solution***
  - **0.007” (175 µm) Pad diameter & 0.004” (100 µm) laser drill**

Pad diameters are driven by device pitch, drill diameter driven by dielectric thickness

0.5 mm BGA

Design Guidelines

IPC 6012 / 6016

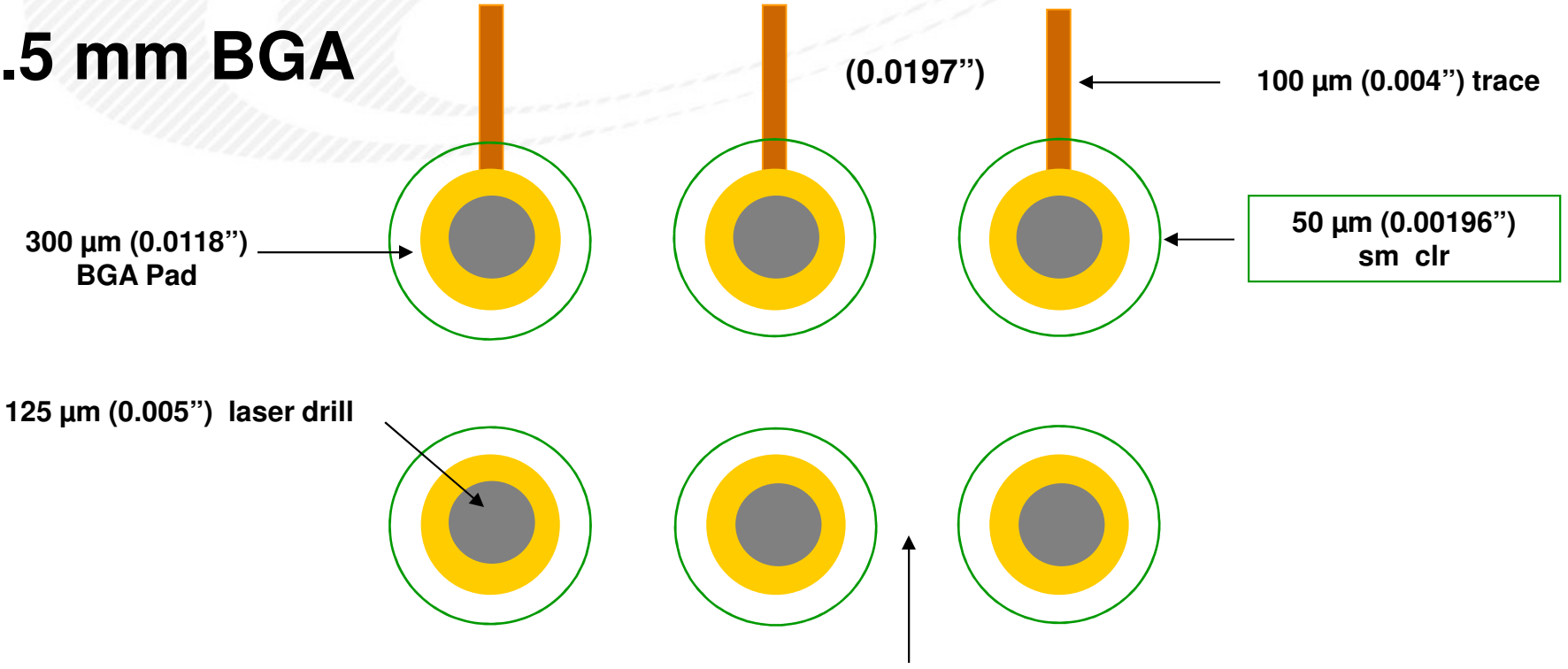
Class 2 & 3

0.5 mm Pitch Guidelines

- 0.5 mm Pitch BGAs require the use of Microvia Technology
- Mechanical drilled through-hole Technology is not an option
- Mechanical Drill violates IPC 6012 fabrication guidelines
- Drill-to-copper is not sufficient and excessive break-out can occur
- Microvias can be used as Via-in-Pad with a solid copper plate
- Microvias can be off-set and staggered

Option A - Preferred

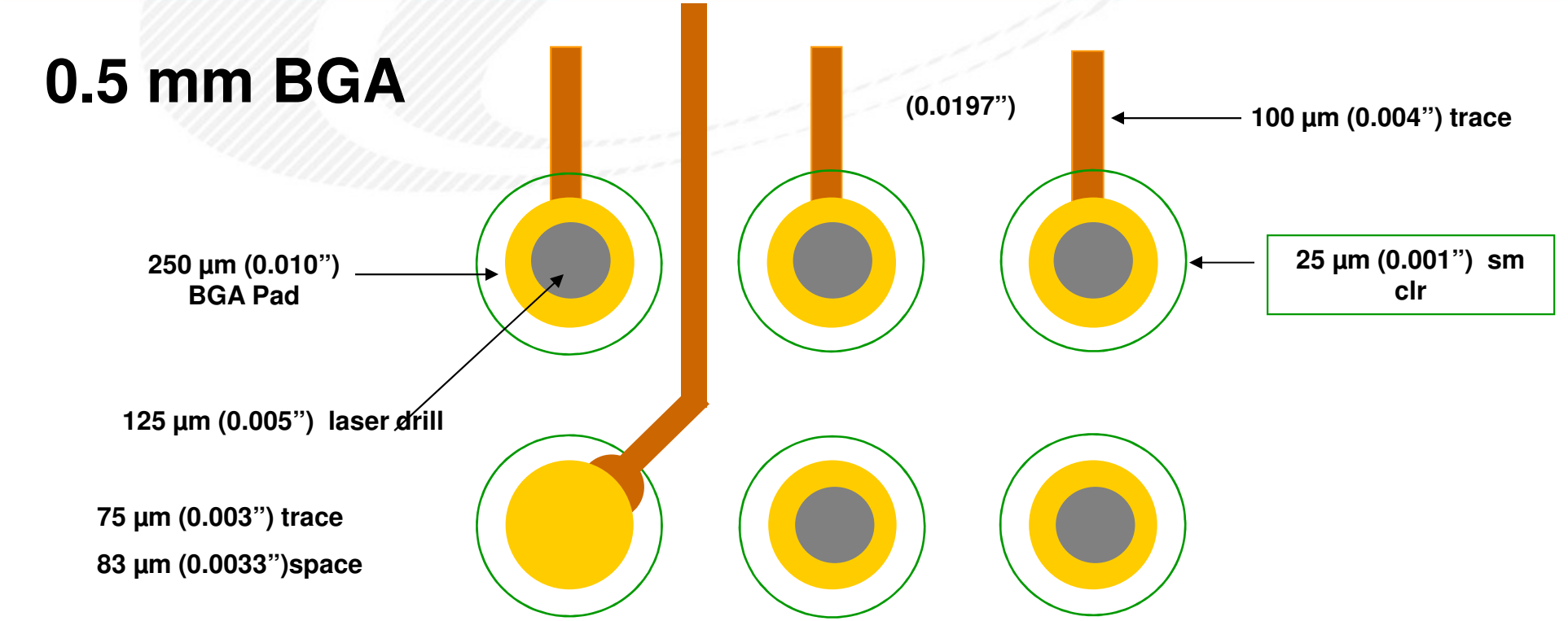
0.5 mm BGA



Utilize Microvia SMV® Technology

External

Option B adds cost & LDI Solder Mask



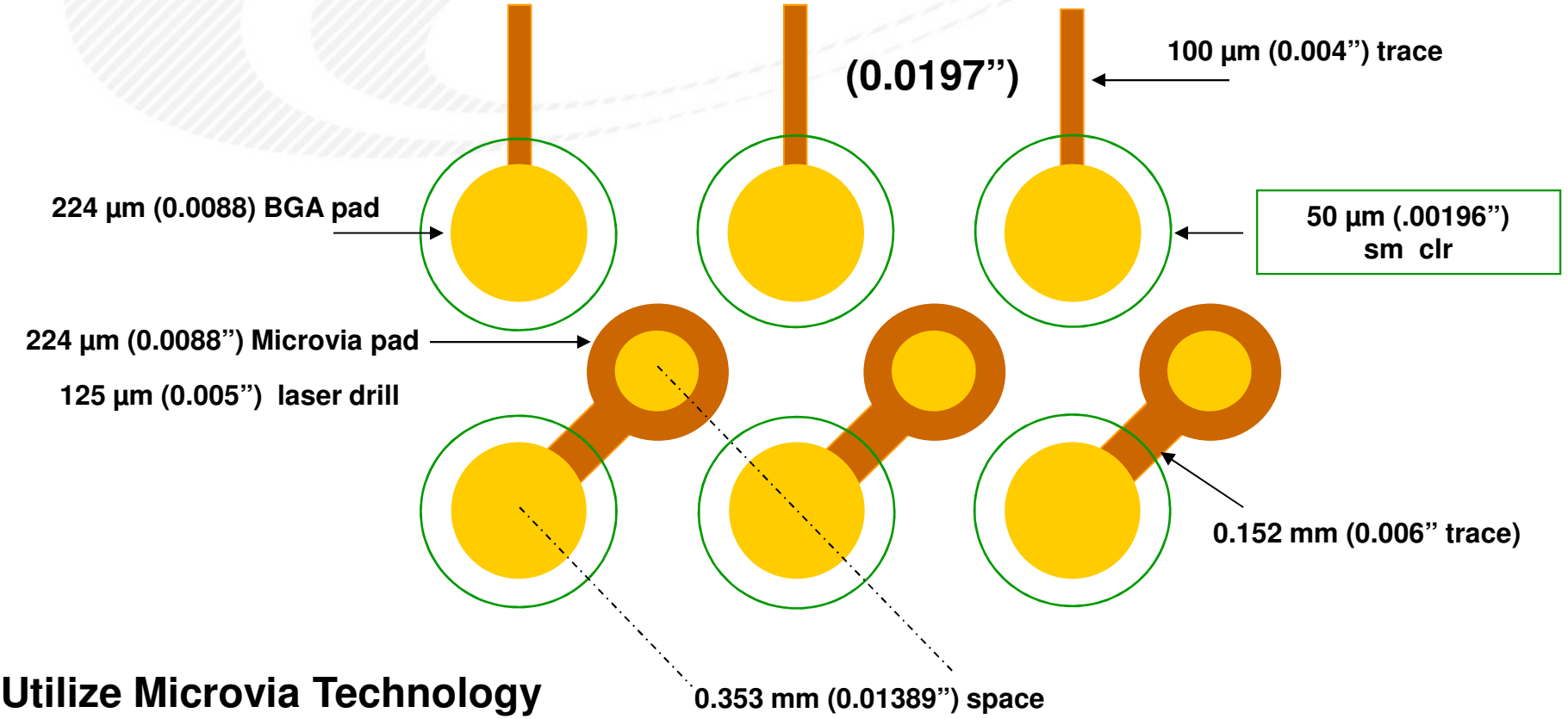
Utilize Microvia SMV® Technology

Requires LDI Solder Mask +/- 25 µm (0.001")

External

Option C reduces cost due to offset

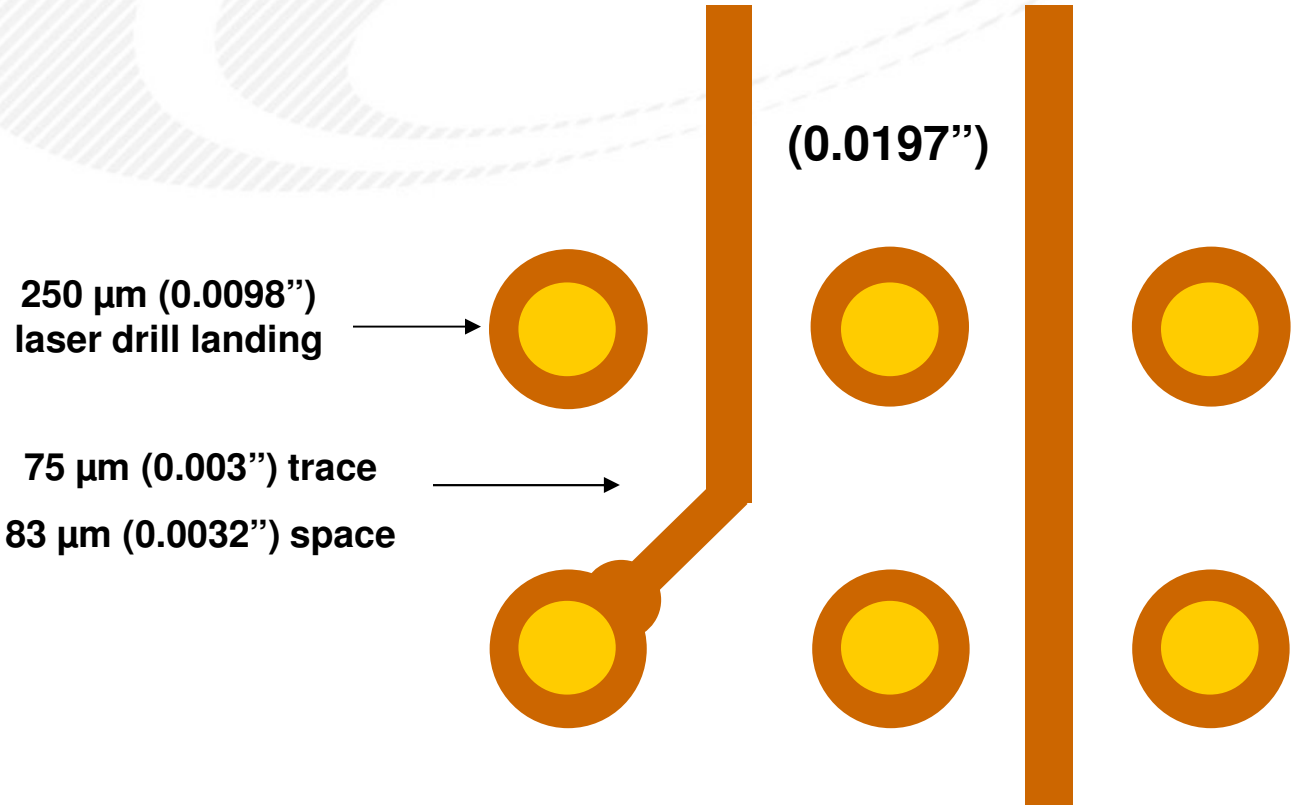
Dog-Bone or Offset Microvia



Utilize Microvia Technology

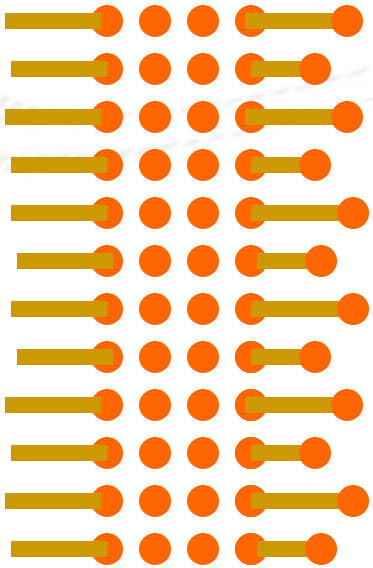
External

0.5 mm BGA



Internal

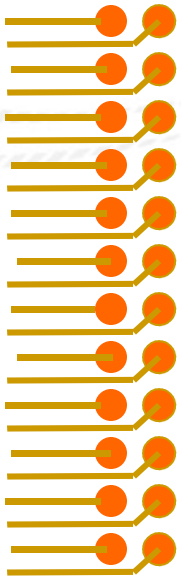
Microvia Technology - 4 Row 256 I/O



Rout outside row on Layer 1

Inside row “inside” to staggered through-vias

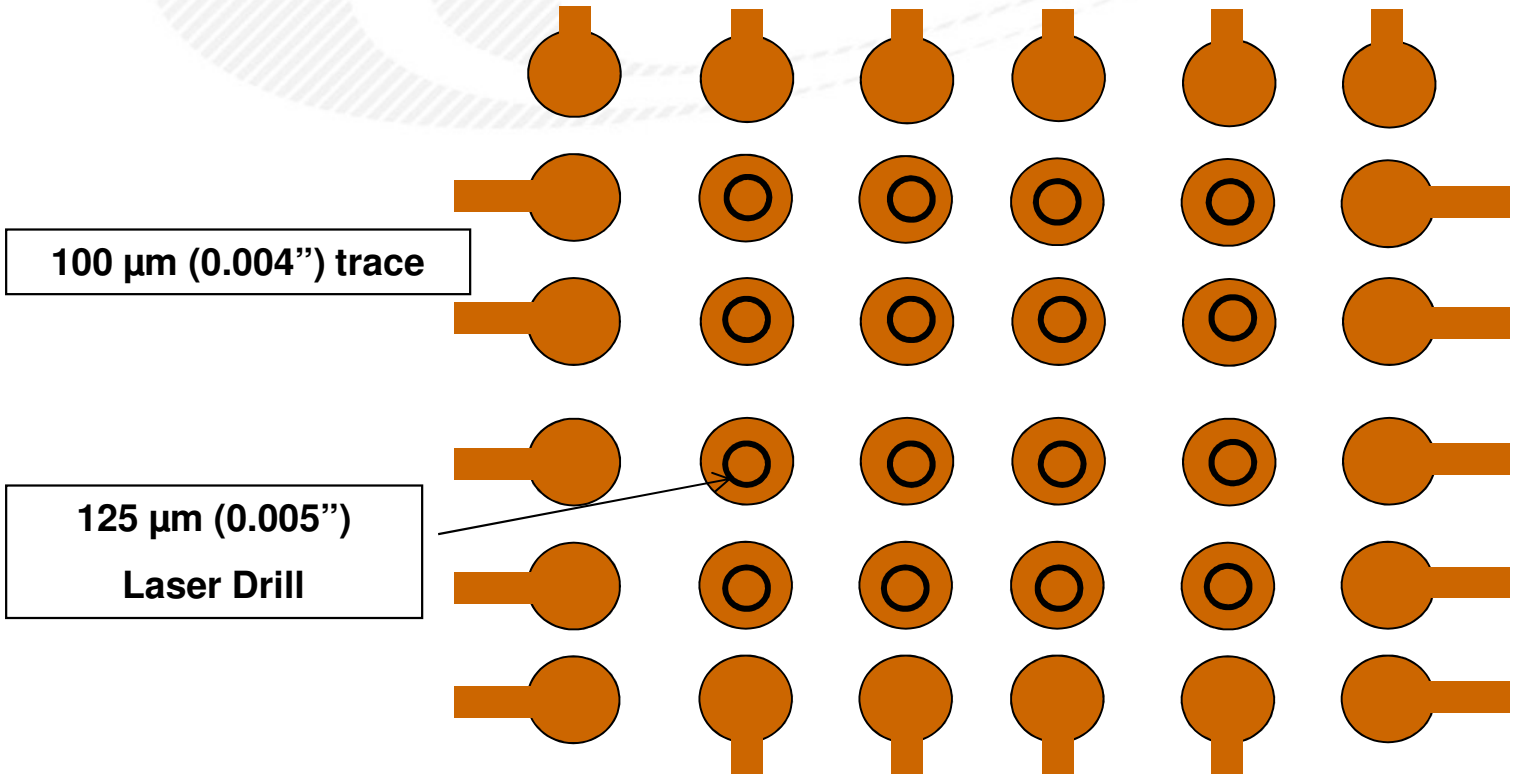
Microvia Technology - 4 Row 256 I/O



Second Row is now outside row on Layer 2

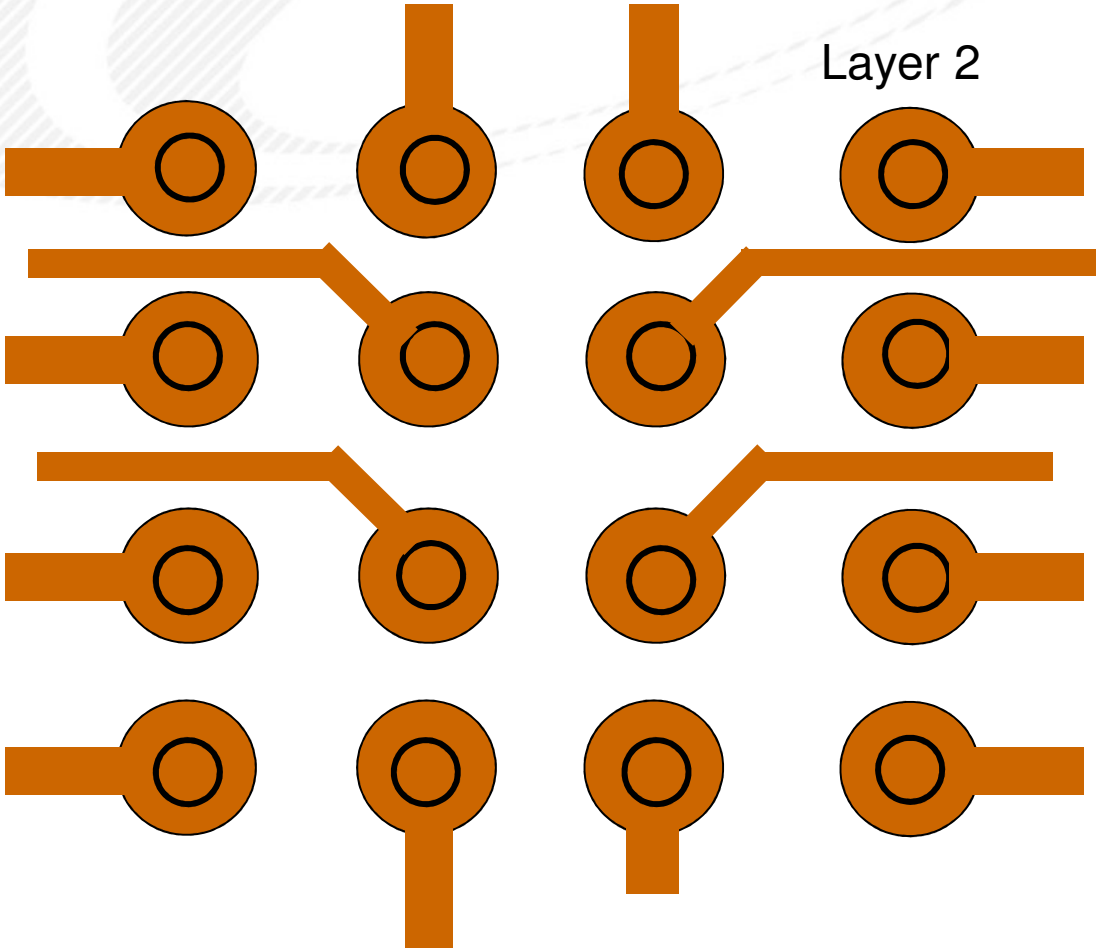
Rout row 2 & 3

0.5 mm BGA Design 6 x 6



Layer 1

0.5 mm BGA Design 6 x 6



1 Track Routing

0.003” (75 µm) trace

0.0033” (83 µm) space

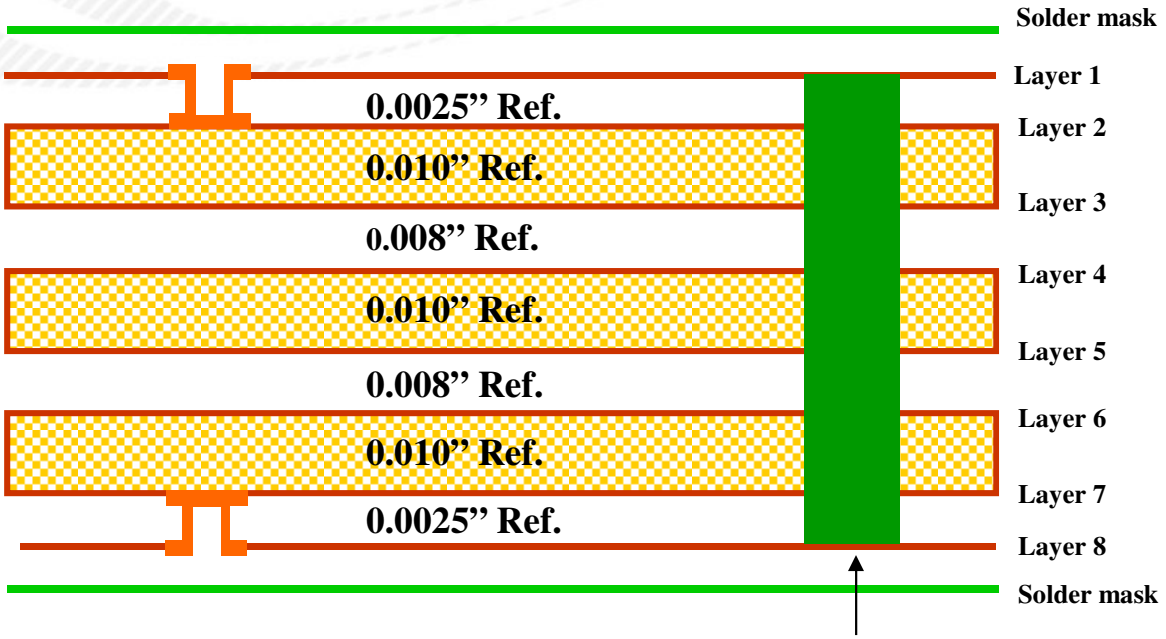
0.010” (250 µm) pad

Lowest cost due to one lamination cycle

Dog-Bone or Offset Microvia

1 + 6 + 1

Offset Microvias
Layer 1 - 2
Layer 8 - 7
0.010” pad
0.005” laser drill



Finish Thickness = 0.062” +/- 0.007”
Material = High Temp FR4

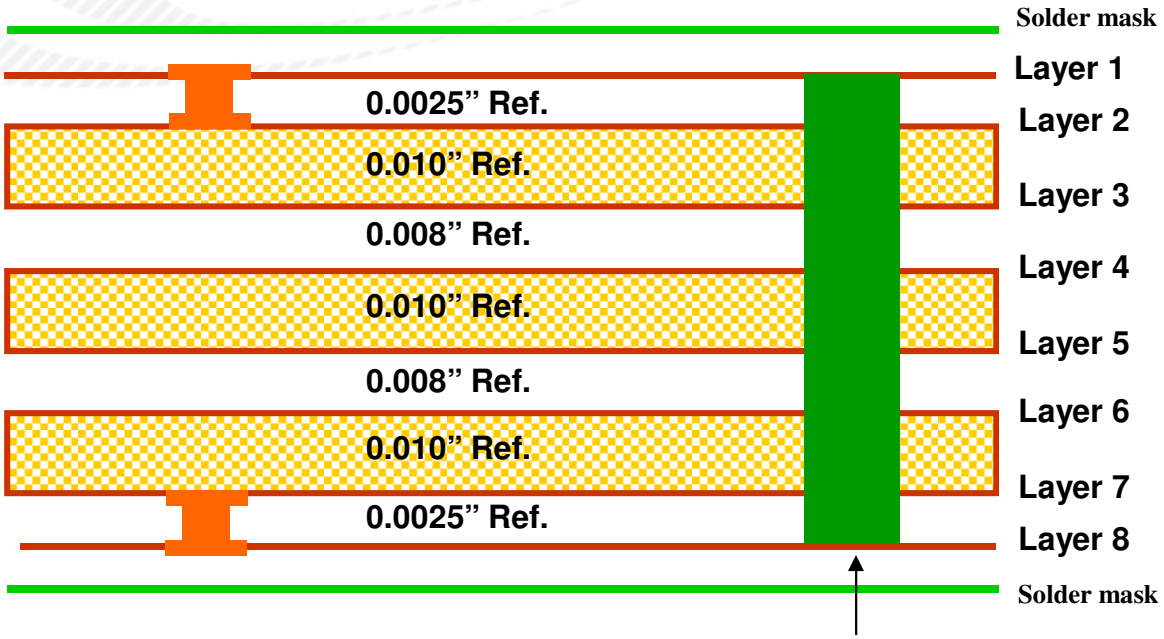
Layer 1 – 8 through vias
0.018” pad & 0.008” drill

Lowest cost due to one lamination cycle

Via-in-Pad with solid copper Plate

1 + 6 + 1

Microvias Via-in-pad
Layer 1 - 2
Layer 8 - 7
0.010” pad
0.005” laser drill



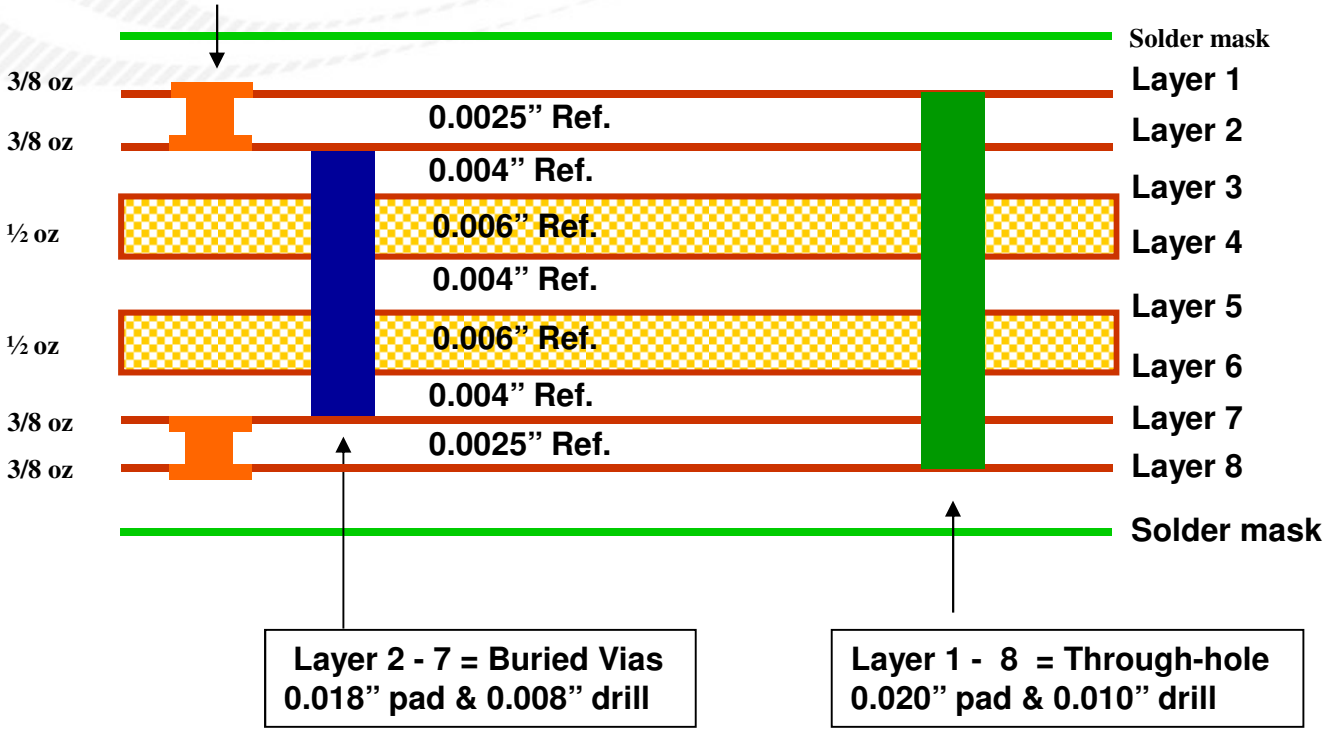
Finish Thickness = 0.062” +/- 0.007”
Material = High Temp FR4

Layer 1 – 8 through vias
0.018” pad & 0.008” drill

Adds cost due to Additional Processing

Two Lamination, Drill & Plating cycles

Layer 1 - 2 & 8-7 - Microvias via-in-pad
L1 0.010” pad & 0.005” laser drill



Layer 2 - 7 = Buried Vias
0.018” pad & 0.008” drill

Layer 1 - 8 = Through-hole
0.020” pad & 0.010” drill

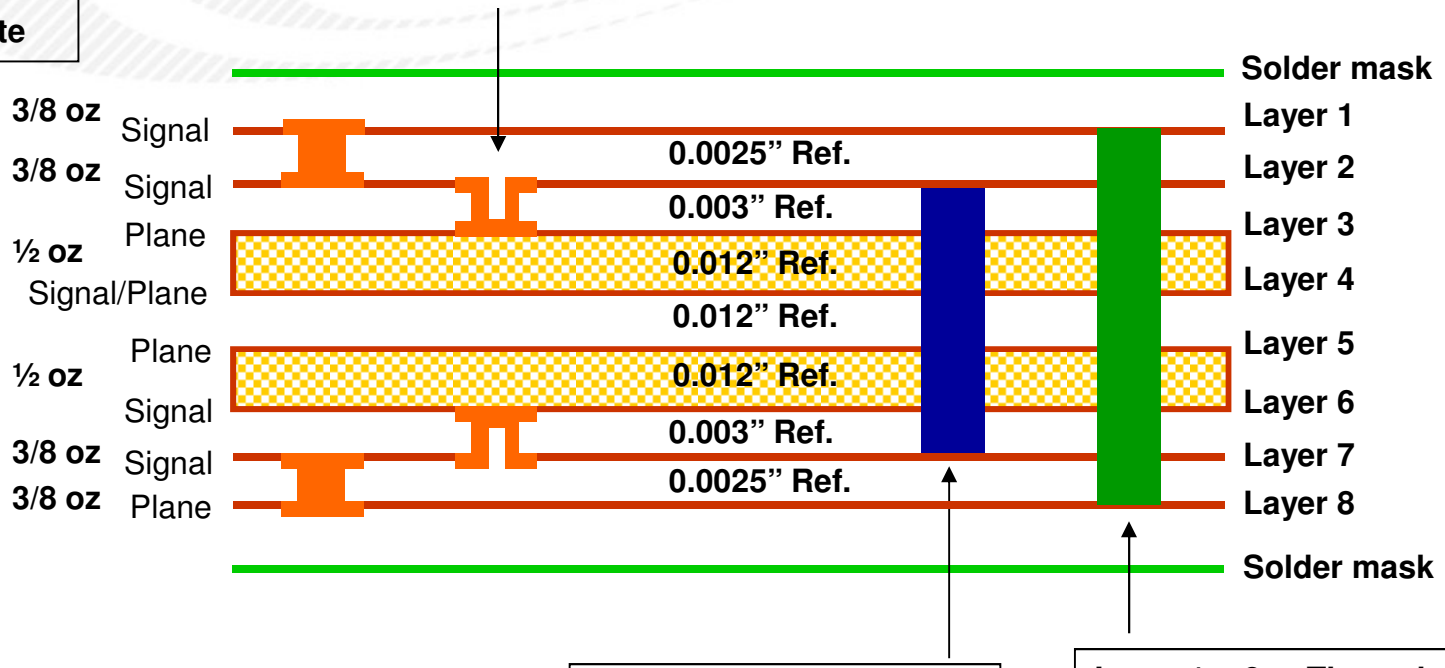
Finish Thickness = 0.042” +/- 0.005”

Adds cost due to Additional Processing

Via-in-Pad & Offset Microvias

MicroVias Via-in-Pad
1-2 & 8 - 7
0.010” pad
0.005” laser drill
Solid Copper Plate

Layer 2 - 3 & 7 – 6 = Offset Microvias
0.010” pad & 0.005” laser drill



Layer 2 - 7 = Buried Vias
0.018” pad & 0.008” drill

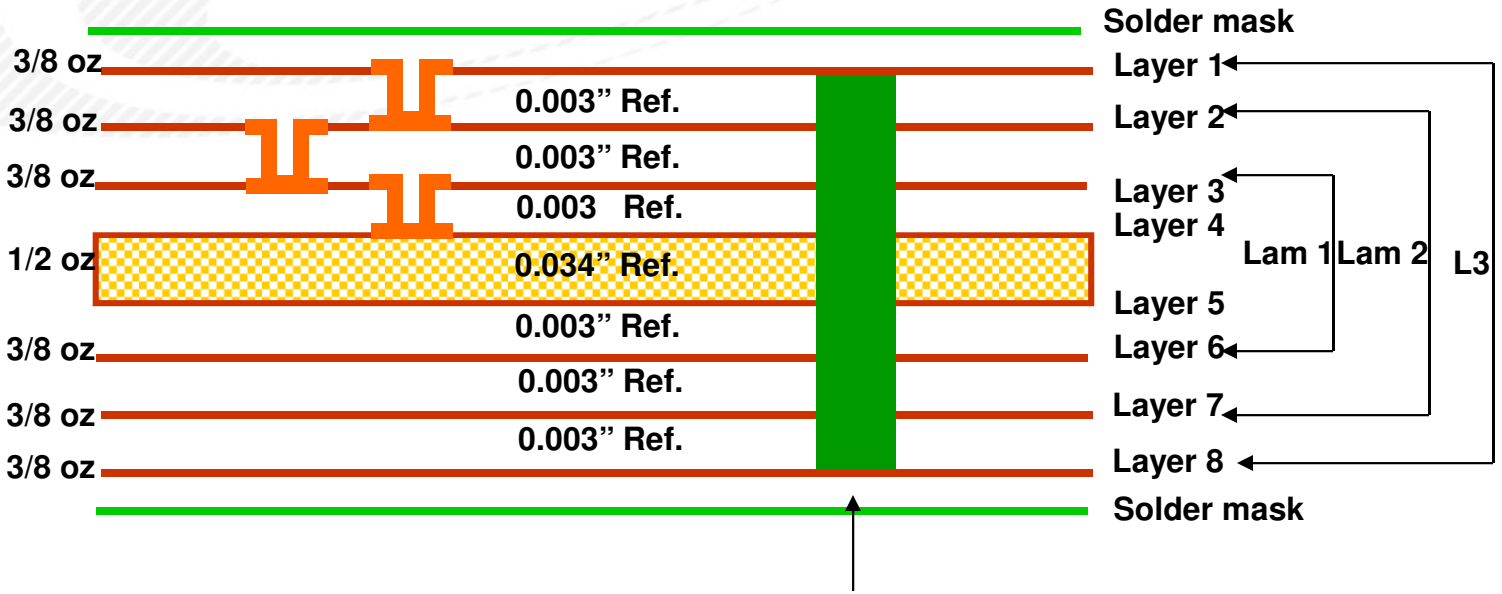
Layer 1 - 8 = Through-hole
0.018” pad & 0.008” drill

Finish Thickness = 0.062” +/- 0.007”
Material = High temp FR4

Lower Cost for 0.5 mm pitch or greater

Dog-Bone & Offset Microvia

Offset Microvias
Layer 1 - 2 & 2 - 3
3 - 4
0.010” pad
0.005” laser drill



Through-Hole Via
0.018” pad
0.008” drill

Finish Thickness = 0.063” +/- 0.007”
Material = High Temperature FR4

0.4 mm BGA

Design Guidelines

IPC 6012 / 6016

Class 2 & 3

0.4 mm Pitch Guidelines

- 0.4 mm Pitch BGAs require the use of Microvia Technology
- Mechanical drilled through-hole Technology is not an option
- Mechanical Drill violates IPC 6012 fabrication guidelines
- Drill-to-copper is not sufficient and excessive break-out can occur
- Microvias can be used as Via-in-Pad with a solid copper plate
- Microvias (0.4 mm pitch) can not be off-set or staggered
  - Can “Dog-Bone” to a buried via

SMV™ Technology Capable of multiple layers

0.4 mm BGA

Design Guidelines:

- ***Standard SMV®***

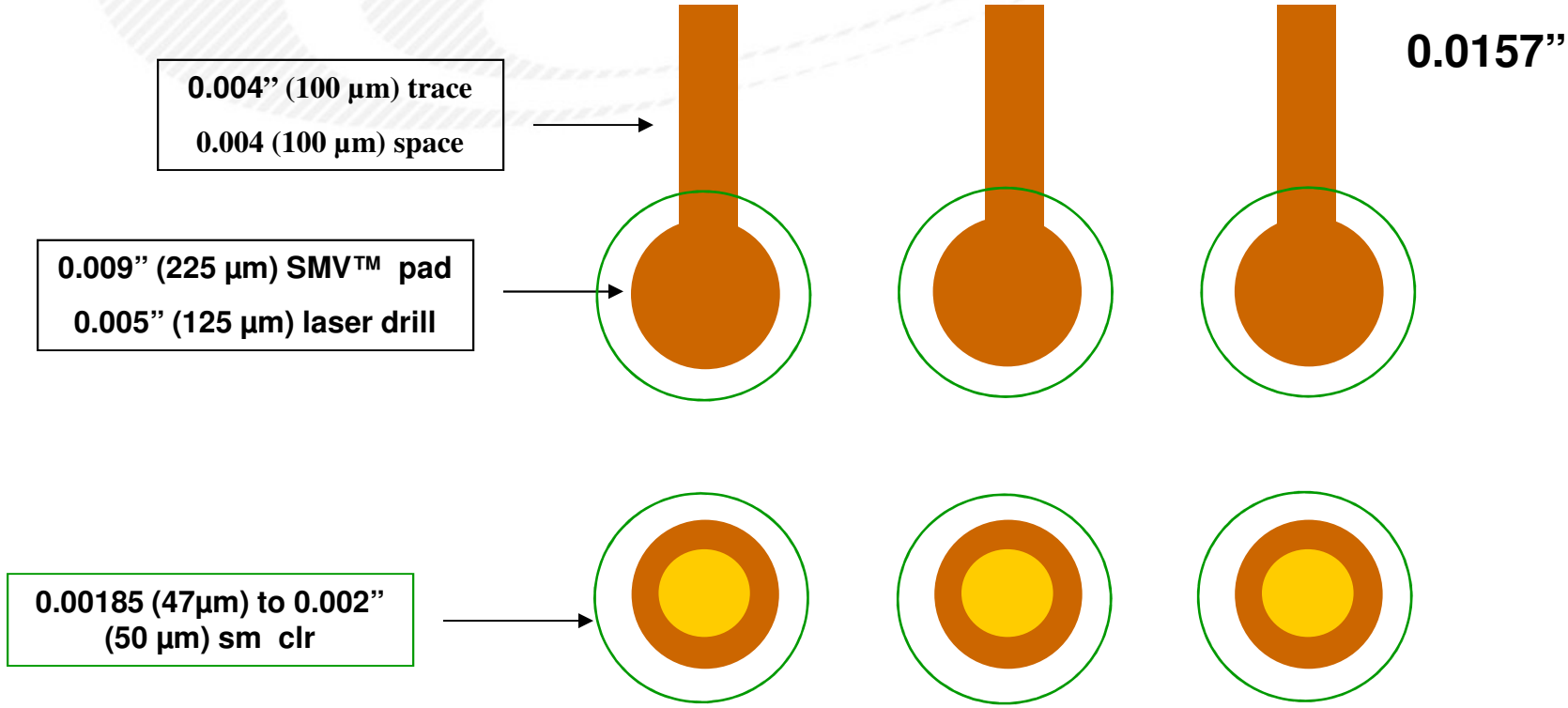
➢ **0.009” (225 µm) external & 0.011” internal (275 µm) Pad diameter & 0.005” (125 µm) laser drill**

- ***Advanced SMV® (cost adder)***

➢ **0.009” (225 µm) external & 0.0086” internal (218 µm) Pad diameter & 0.005” (125 µm) laser drill**

SMV™ Technology Capable of multiple layers

0.4 mm BGA

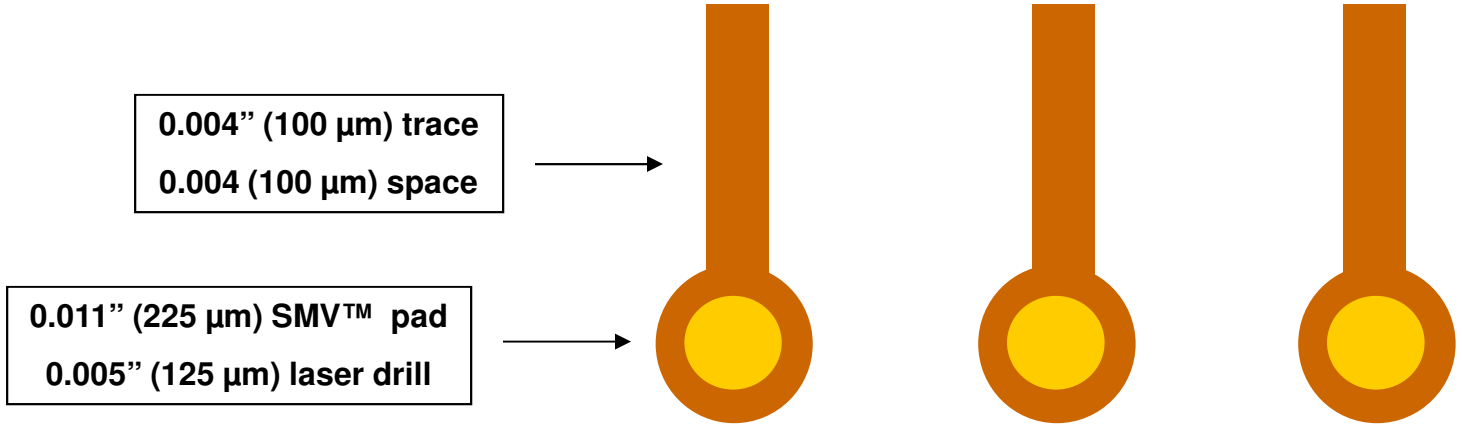


External Layer 1 0.0027” to 0.003” Solder Dam

SMV™ Technology Capable of multiple layers

0.4 mm BGA

0.0157”



Internal Layer 2 – second row is outside row

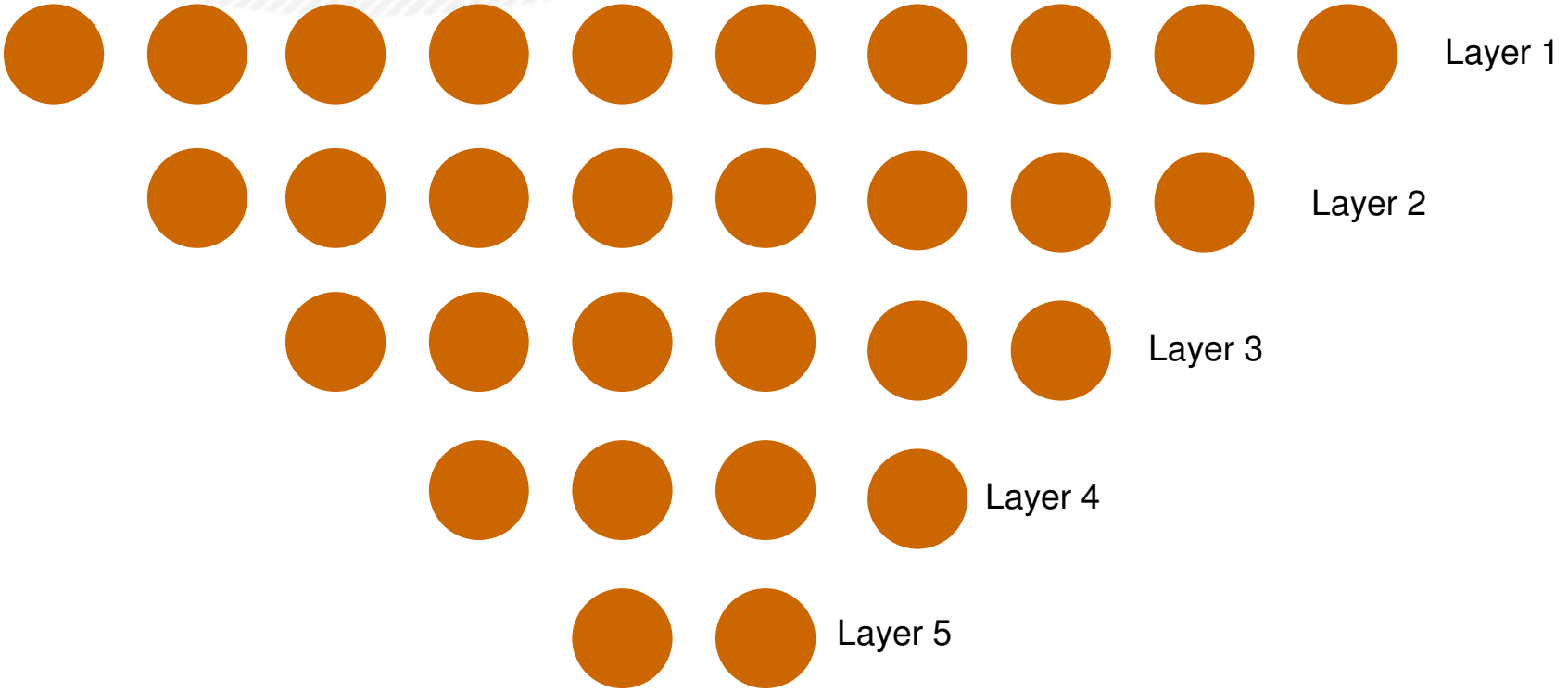
Continue to fan out outside row and use Inverted Pyramid approach

Layer 3 - 4 - 5

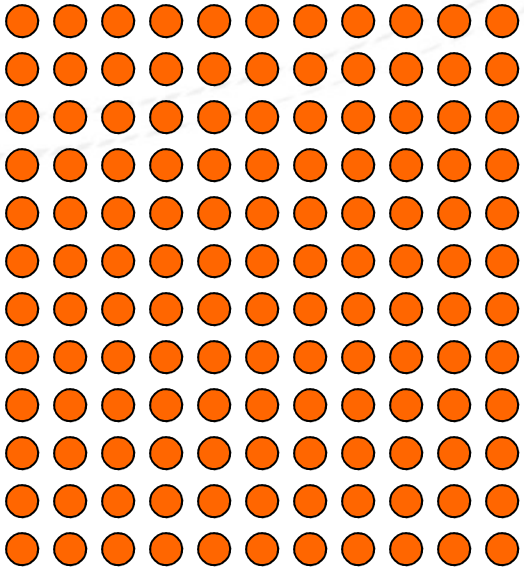
Example of Inverted Pyramid Routing

0.4 mm Pitch Fan out

Inverted Pyramid

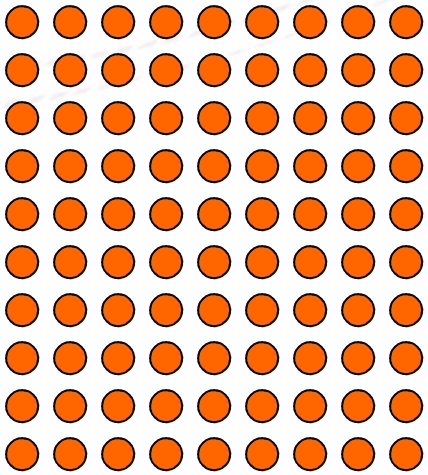


12 X 11 0.4 mm pitch



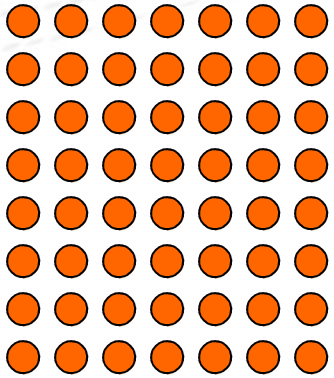
Rout outside row on Layer 1

12 X 11 0.4 mm pitch



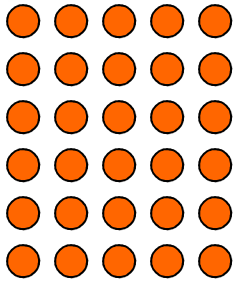
Rout outside row on Layer 2

12 X 11 0.4 mm pitch



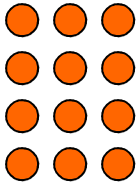
Rout outside row on Layer 3

12 X 11 0.4 mm pitch



Rout outside row on Layer 4

12 X 11 0.4 mm pitch



Rout outside row on Layer 5

12 X 11 0.4 mm pitch

Rout outside row on Layer 6

0.4 mm BGA

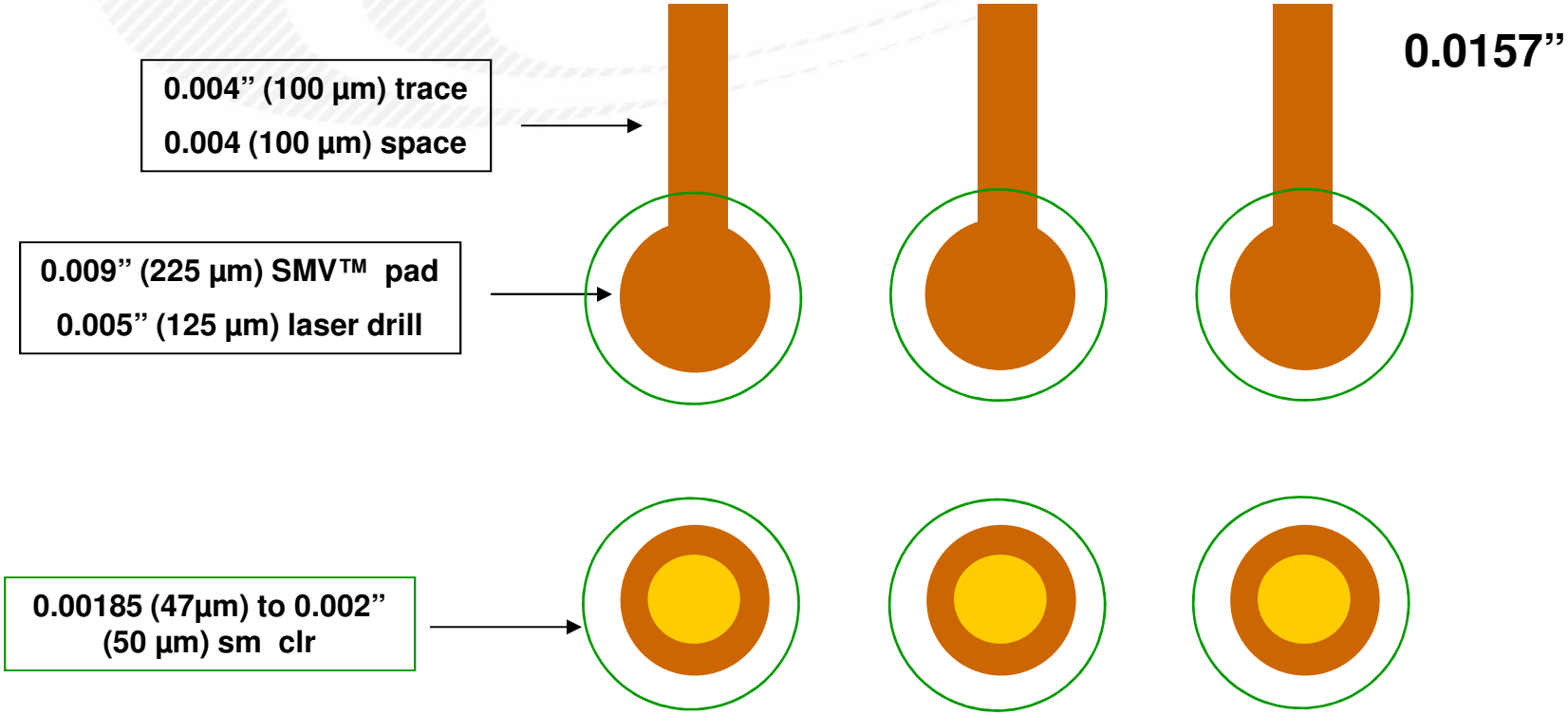
Design Guidelines

Advanced Technology

Adds Cost

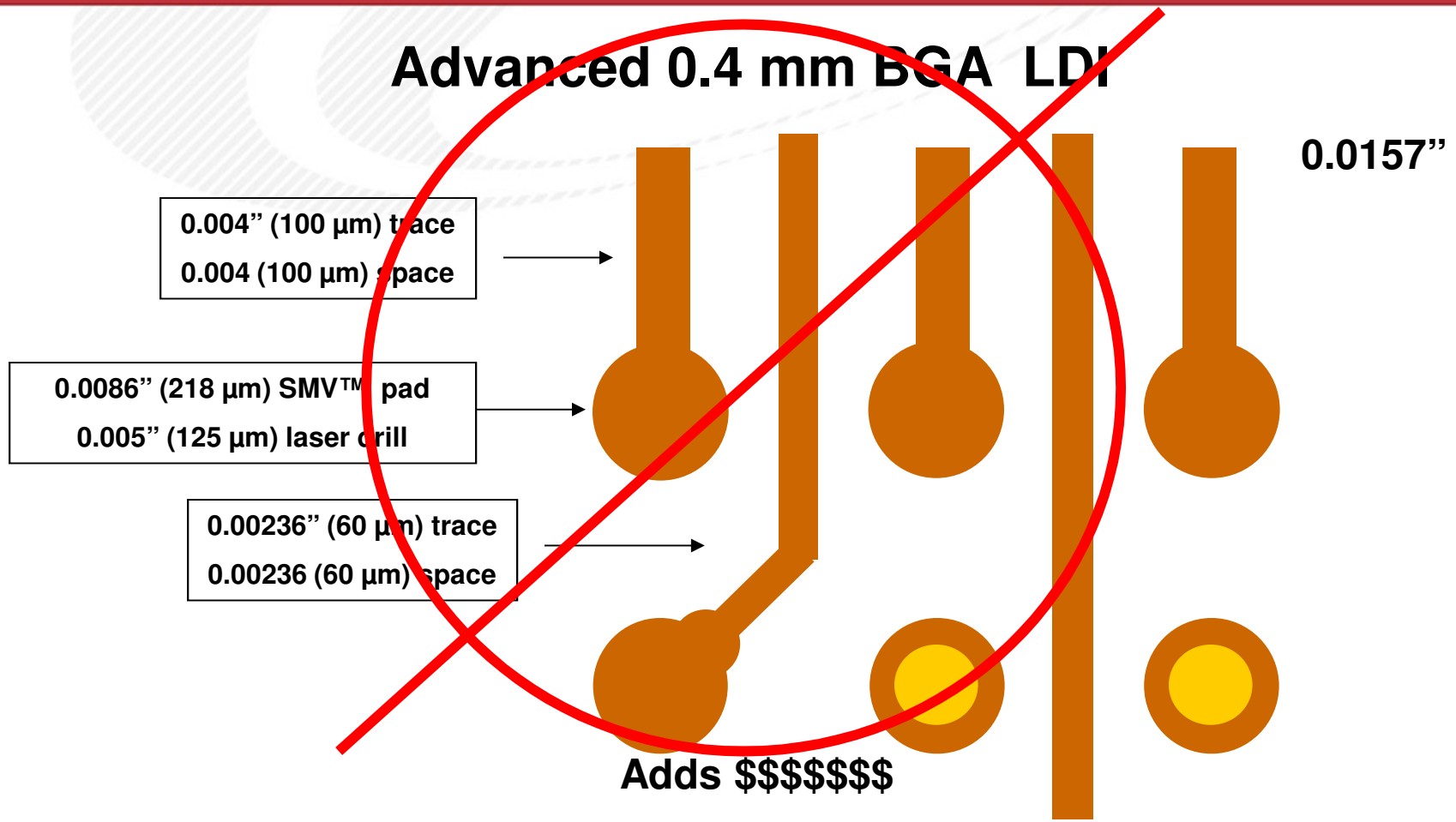
SMV™ Technology Capable of multiple layers

0.4 mm BGA



External Layer 1 0.0027" to 0.003" Solder Dam

SMV™ Technology Capable of multiple layers

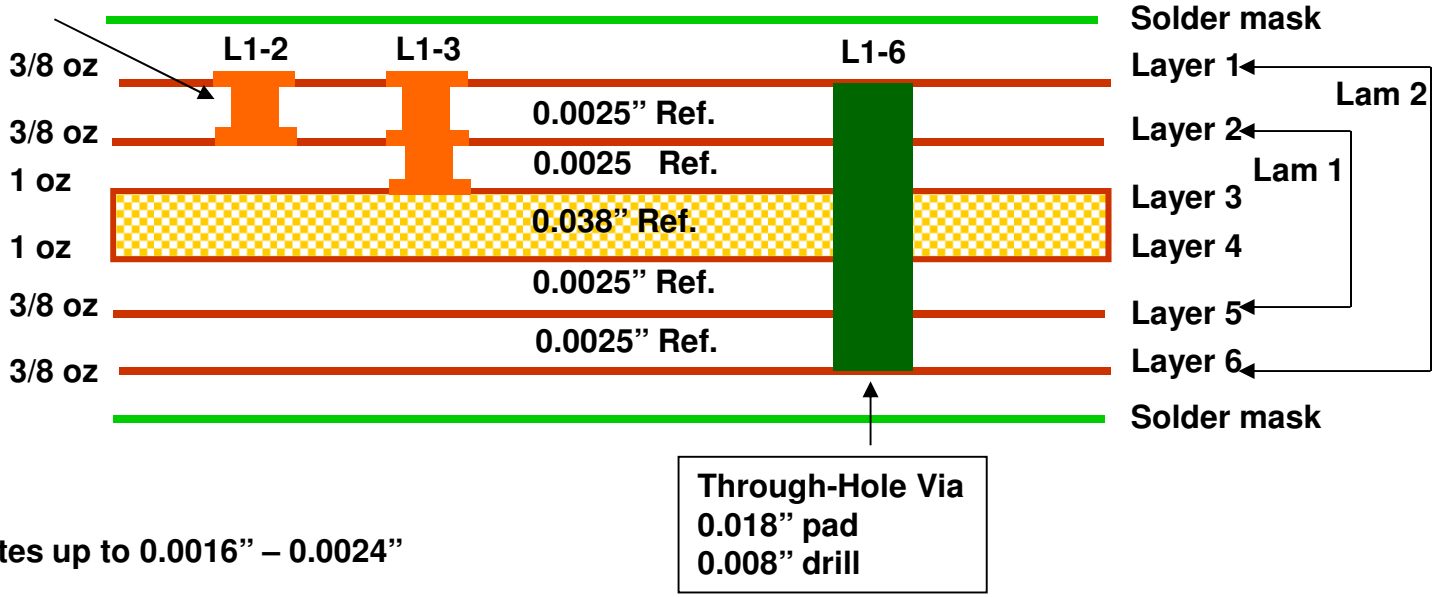


Recommend fan out on each layer using Inverted Pyramid approach

Six Layer SMV® Construction 0.4 mm pitch

Stacked MicroVias
Layer 1 - 2 & 2 - 3
0.009" external
0.011" pad internal
0.005" laser drill
Solid Copper Plate

Two plating, drilling, & Lamination Cycles,



Through-Hole Via
0.018" pad
0.008" drill

3/8 oz copper plates up to 0.0016" – 0.0024"

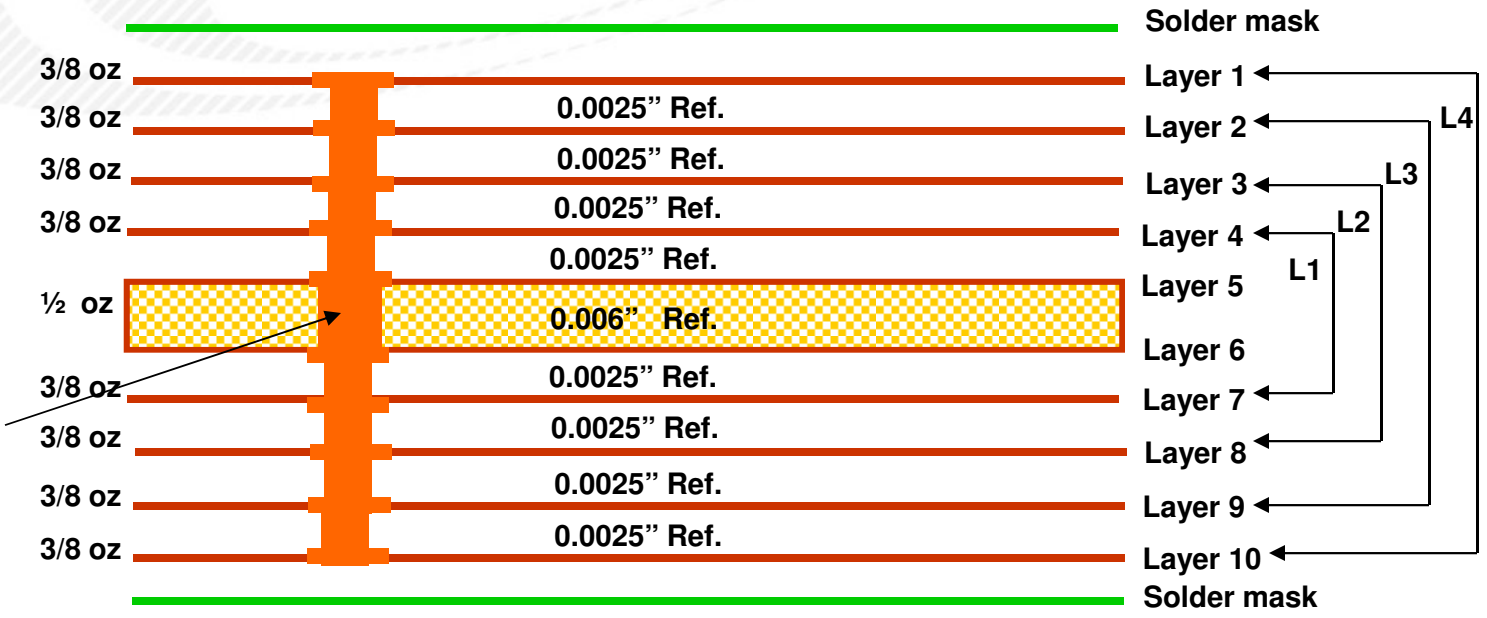
Finish Thickness = 0.062" +/- 0.007"
Material = High Temperature FR4

Ten Layer "Full Stack" SMV®

Stacked MicroVias
Layer 1 - 2
Layer 2 – 3
Layer 3 – 4
Layer 8 - 7
Layer 7 – 6
Layer 6 - 5
0.0011" pad
0.005" laser drill
Solid Cu Plate

Buried Via
Layer 4 - 5
0.012" pad
0.006" mech drill
Solid cu plate
or laser drill
Solid cu plate

0.4 mm Pitch



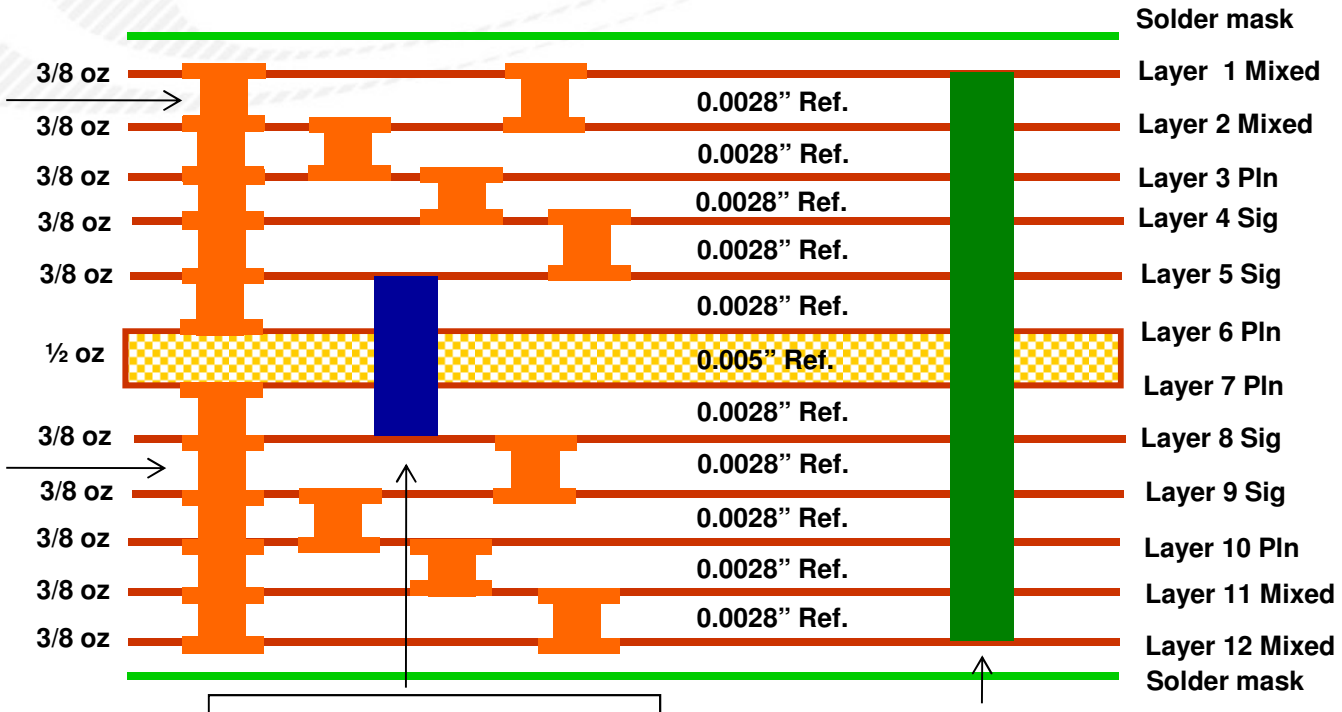
Finish Thickness = 0.045" +/- 0.005"
Material = High Temperature FR4

Stacked MicroVia (SMV®)

VIASYSTEMS.

Stacked MicroVias
Layer 1 - 2
Layer 2 - 3
Layer 3 – 4
Layer 4 – 5
Layer 5 – 6
0.011” pad internal
0.005” laser drill
Solid copper plate

0.4 mm BGA Advanced Construction



Stacked MicroVias
Layer 13 – 12
Layer 12 – 11
Layer 11 – 10
Layer 10 – 9
Layer 9 - 8
0.011” pad internal
0.005” laser drill
Solid copper plate

Layer 5- 8 = through holes
0.016” pad
0.006” drill

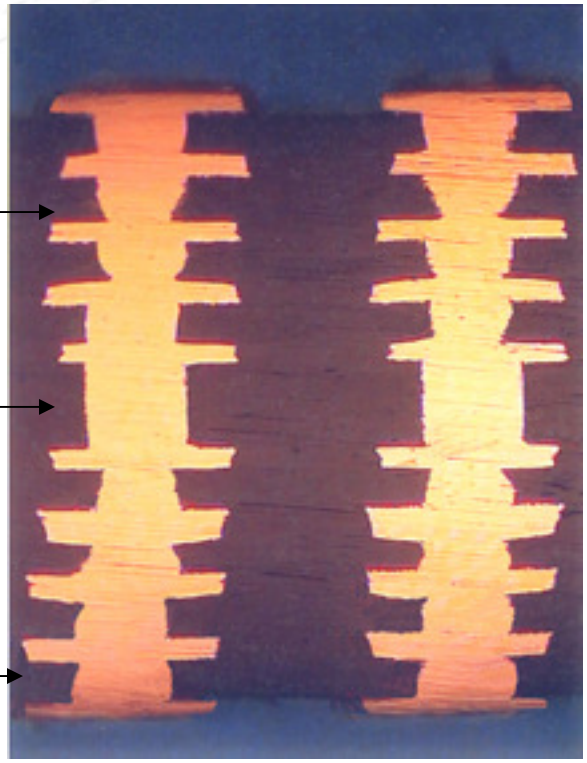
Layer 1- 12 = through holes
0.018” pad
0.008” drill

Finish Thickness = 0.054” +/- 0.005”

“Full Stack” SMV® Example

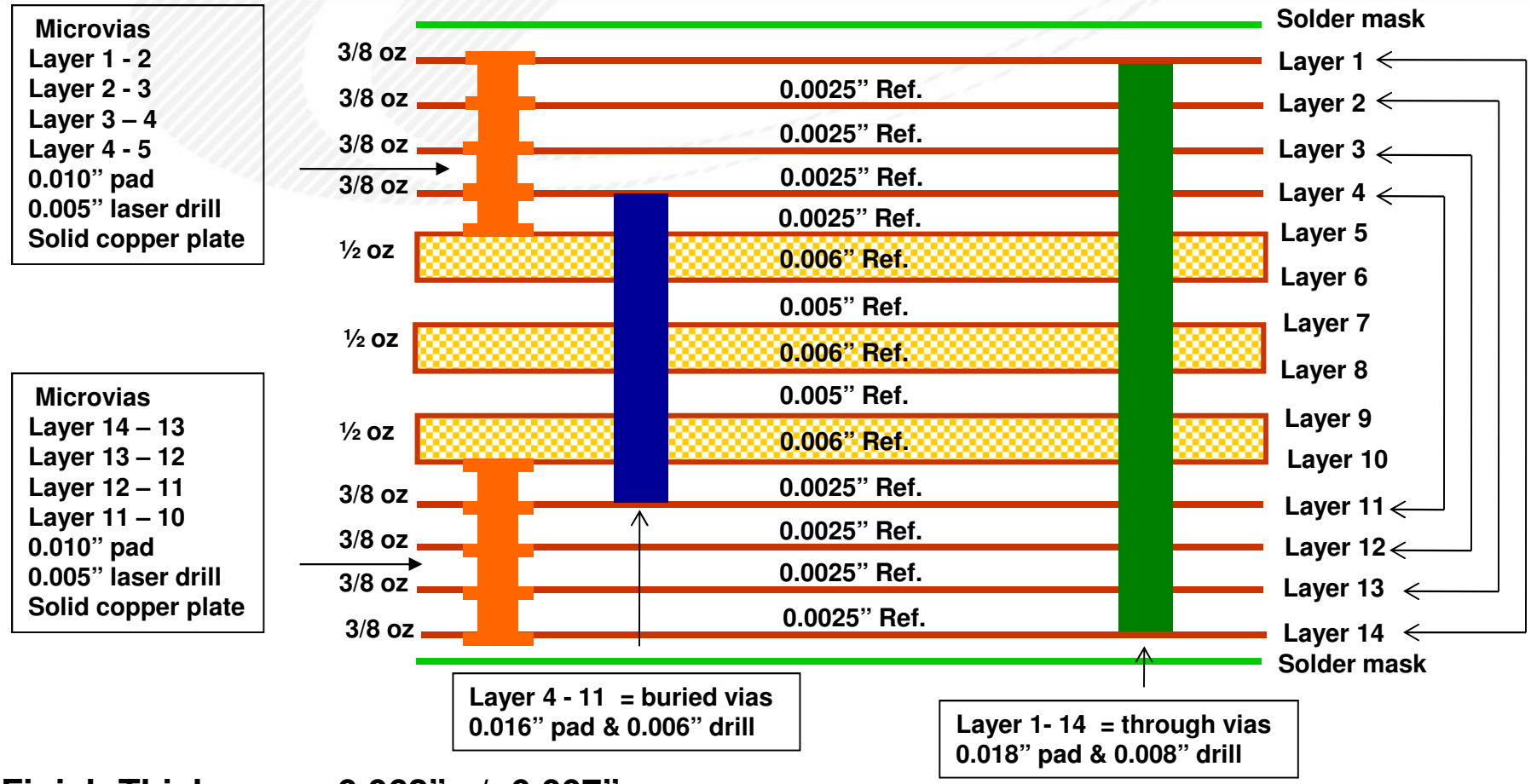
10 Layer SMV™ Technology

Full Build
0.005” (125 µm) Laser drill
0.0025” (64 µm) dielectric
0.006” (150 µm) dielectric
0.006” (150 µm) Mech drill
0.005” (125 µm) Laser drill
0.0025” (64 µm) dielectric
Solid Copper Plate



Core & Microvias = Solid Copper Plate

Fourteen Layer with off-set Buried Via



Finish Thickness = 0.062” +/- 0.007”
Material = High Temperature FR4

0.3 mm BGA

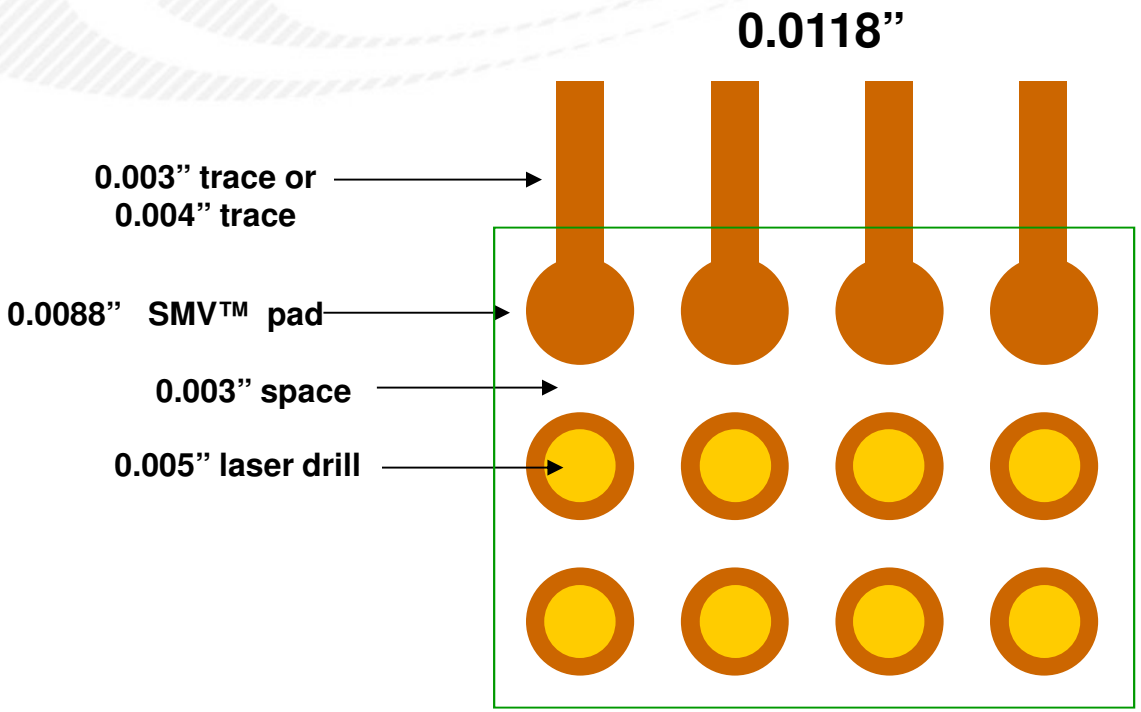
Design Guidelines

IPC 6011 / 6012

Class 2

Stacked MicroVia (SMV®)

0.3 mm Flip Chip

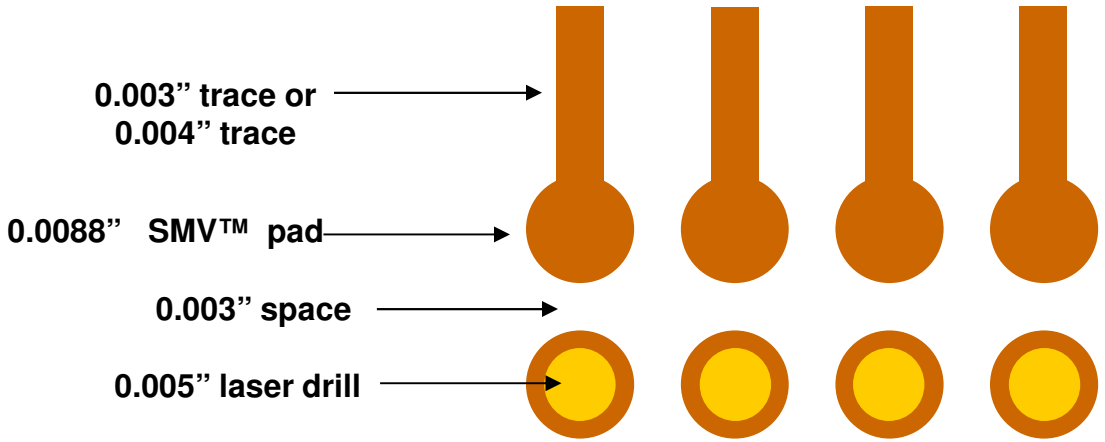


External Layer 1

Stacked MicroVia (SMV®)

0.3 mm Flip Chip

0.0118”

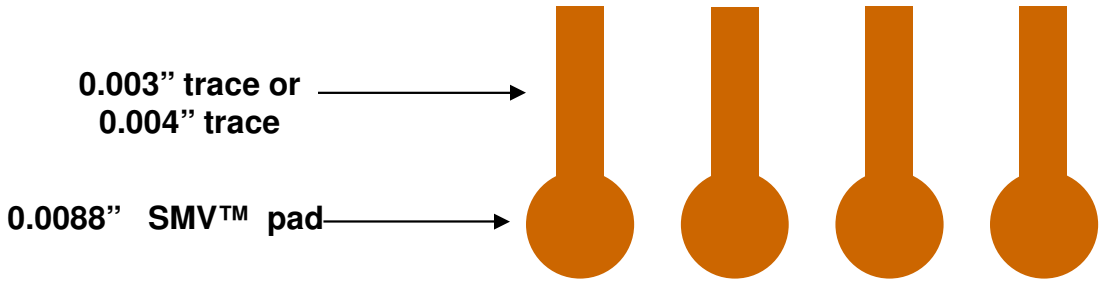


Internal Layer 2

Stacked MicroVia (SMV®)

0.3 mm Flip Chip

0.0118”



Internal Layer 3

0.25 mm BGA

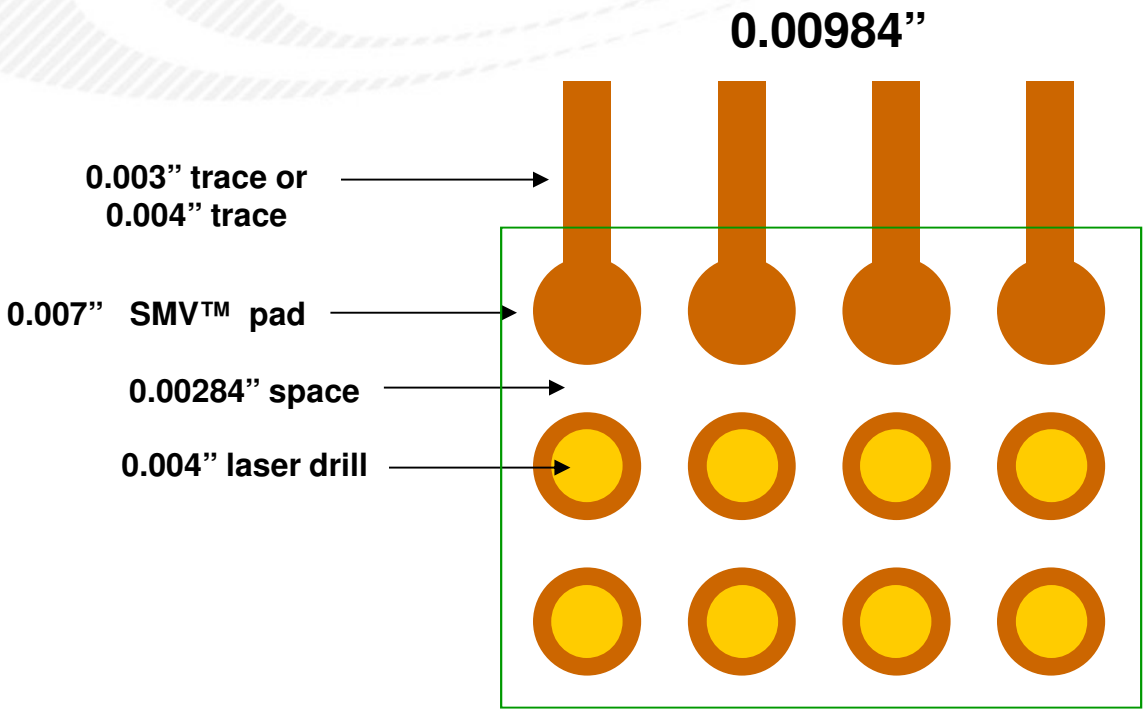
Design Guidelines

IPC 60112/ 6016

Class 2

Stacked MicroVia (SMV®)

0.25 mm Flip Chip

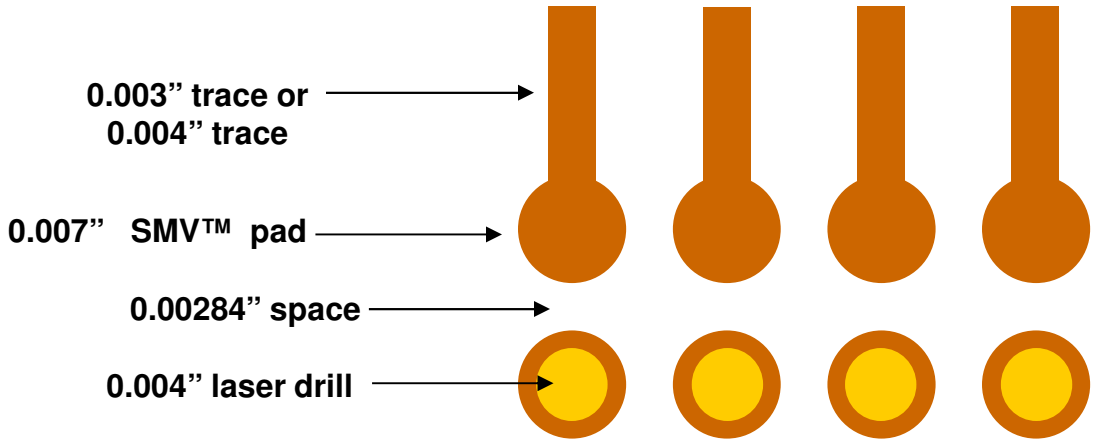


External Layer 1

Stacked MicroVia (SMV®)

0.25 mm Flip Chip

0.00984”

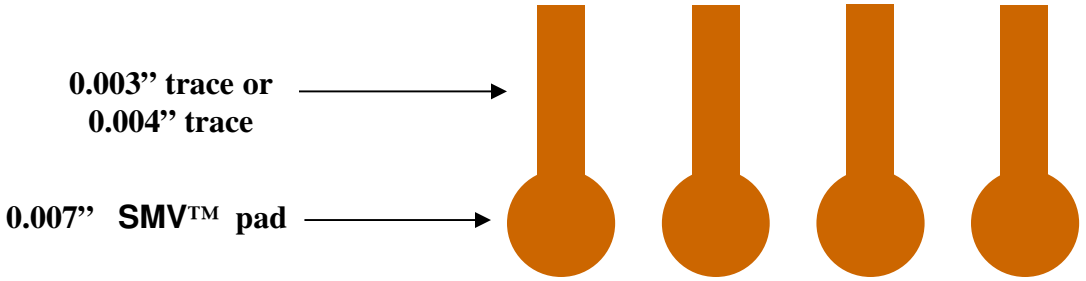


Internal Layer 2

Stacked MicroVia (SMV®)

0.25 mm Flip Chip

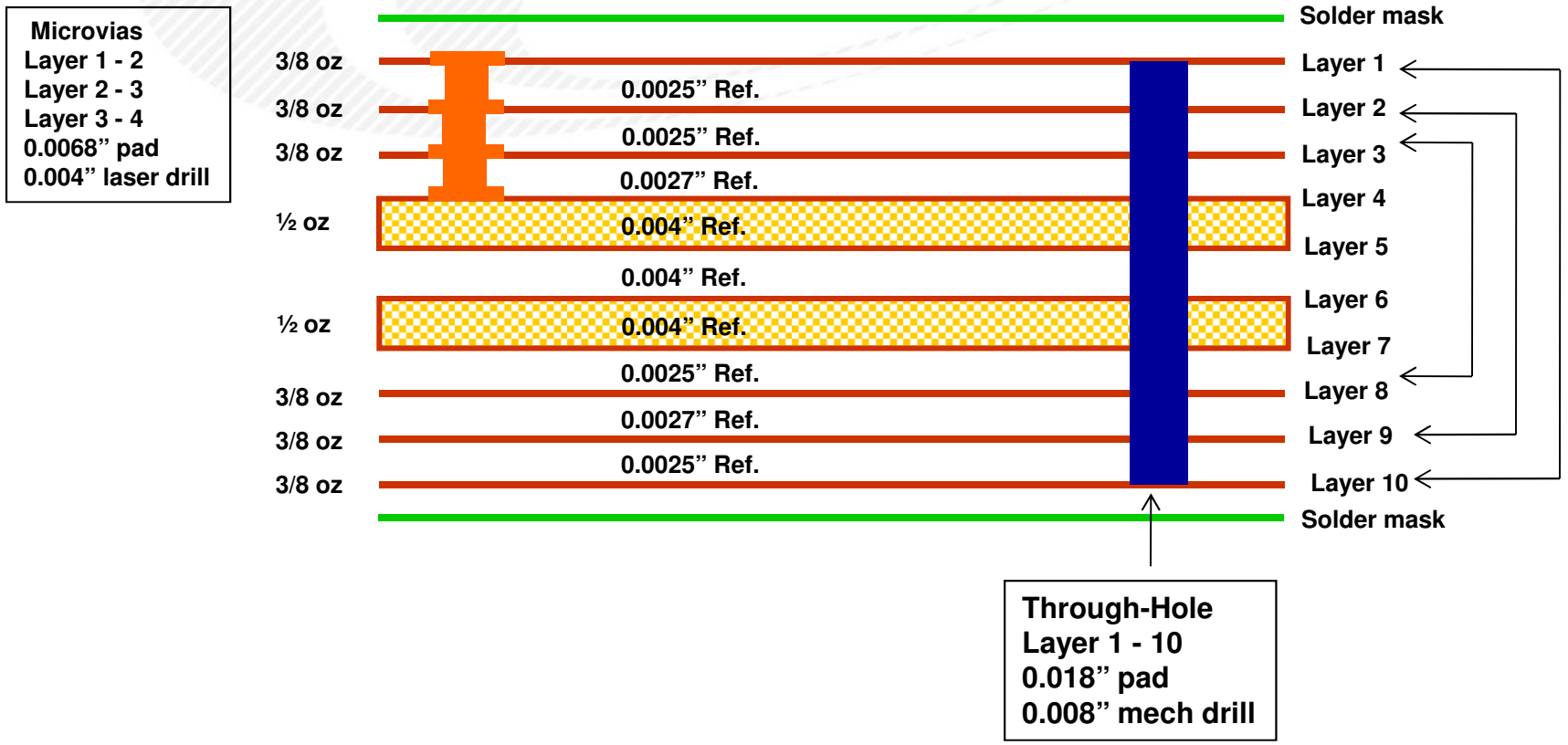
0.00984”



Internal Layer 3

Stacked MicroVia (SMV®)

0.25 mm Pitch

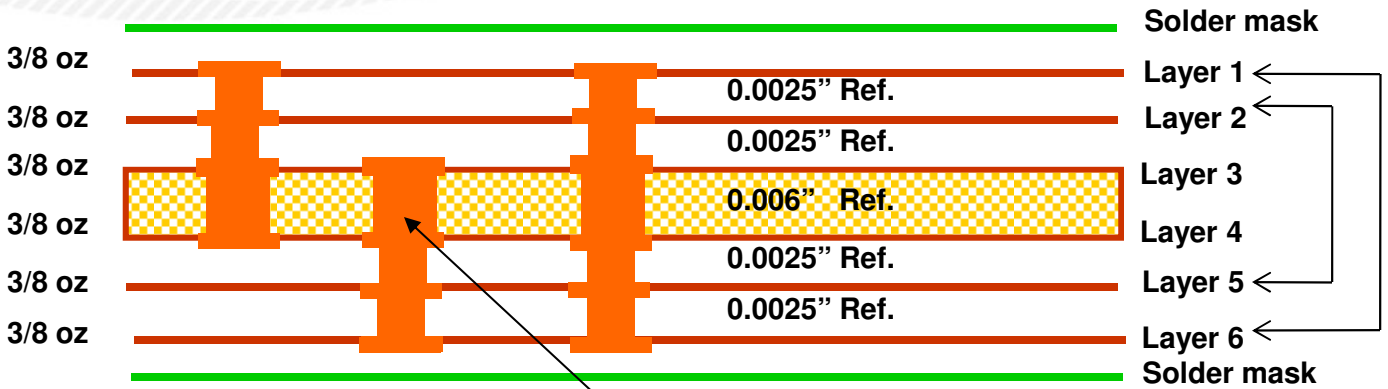


Finish Thickness = 0.044 +/- 0.005
Material = High Temperature FR4

Stacked MicroVia (SMV®)

0.25 mm Pitch

Stacked MicroVias
0.0068" pad
0.004" laser drill
Solid Cu Plate



3/8 oz copper plates up to 0.0016" - .0018"

Buried Via
Layer 3 - 4
0.010" pad
0.006" laser drill
Solid copper plate

Finish Thickness = 0.030" +/- 0.004")
Material = High Temperature FR4

Routing Techniques for Fine Pitch BGAs

- **0.5 mm Pitch – Offset Microvias**
  - External = Dog-Bone Microvias & Staggered Microvias Internal
  - Stacked MicroVias **(SMV®)**
- **0.4 mm Pitch – Stacked MicroVias (SMV®)**
  - Using Inverted Pyramid Technique
- **0.3 mm pitch - Stacked MicroVias (SMV®)**
    - using Inverted Pyramid Technique
- **0.25 mm pitch - Stacked MicroVias (SMV®)**
    - Inverted Pyramid Technique

Microvia Sub-lamination Interface Techniques

Microvia: Sub-Lamination Interface

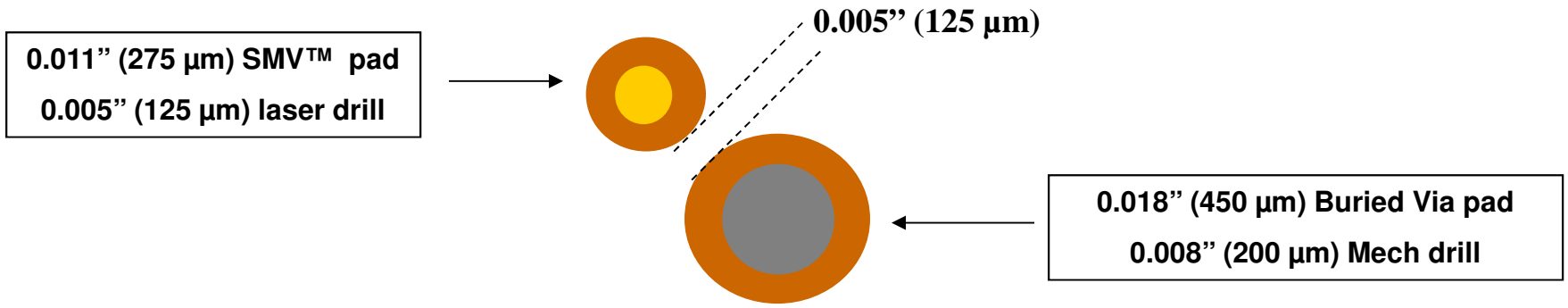
Basic design rules for Microvia build-up layers

- Build-up dielectric layers must be balanced on either side of the sub-lamination
- Build-up dielectric layers are generally 0.0025” (64µm) to 0.003” (75µm) thick
- The recommended total number of lamination cycles that any one part of the structure should experience is 3 and 4 – 5 for advanced structures
- Microvia’s stacked on buried mechanical vias should be avoided due to wrap plating requirements and excessive stress on thicker substrates
- Solid copper mechanically drilled via’s can be used on thin sub-lamination cores in place of wrap plating

Internal Layer "Dog Bone" to a Buried Via - Guidelines

Not a Common Electrical Net

Buried Via Offset Technology for 0.4 mm Pitch

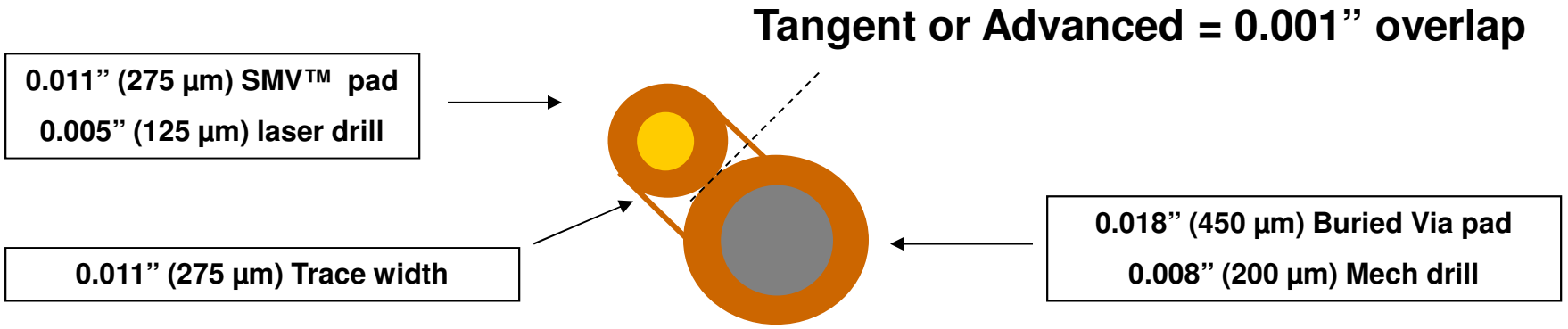


Internal Layer "Dog Bone" to Buried Via

Internal Layer "Dog Bone" to a Buried Via - Guidelines

A Common Electrical Net

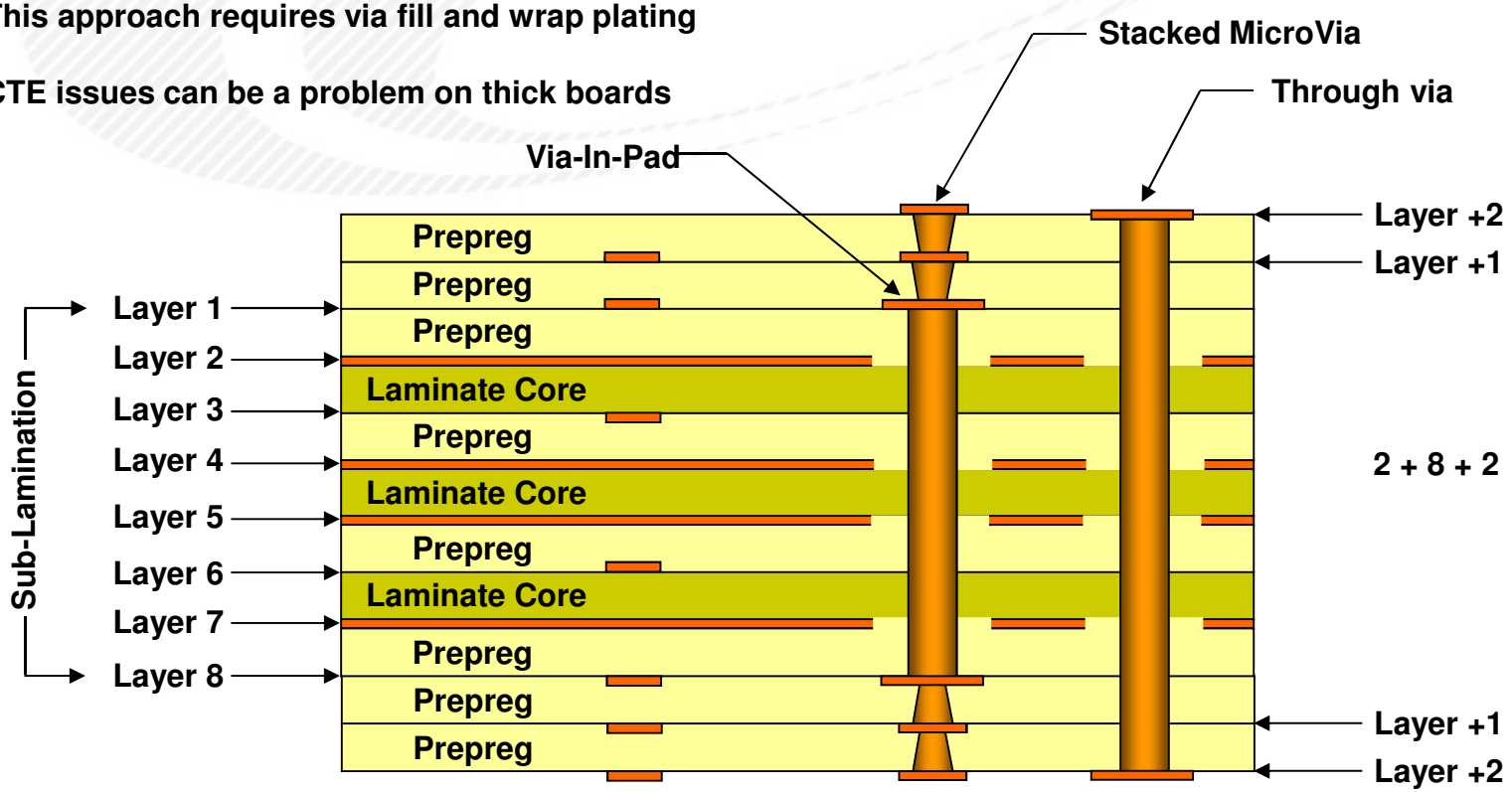
Offset Technology for 0.4 mm Pitch



Internal Layer "Dog Bone" to Buried Via

Microvia Sub-Lamination Interface: Stacked On Sub-Via

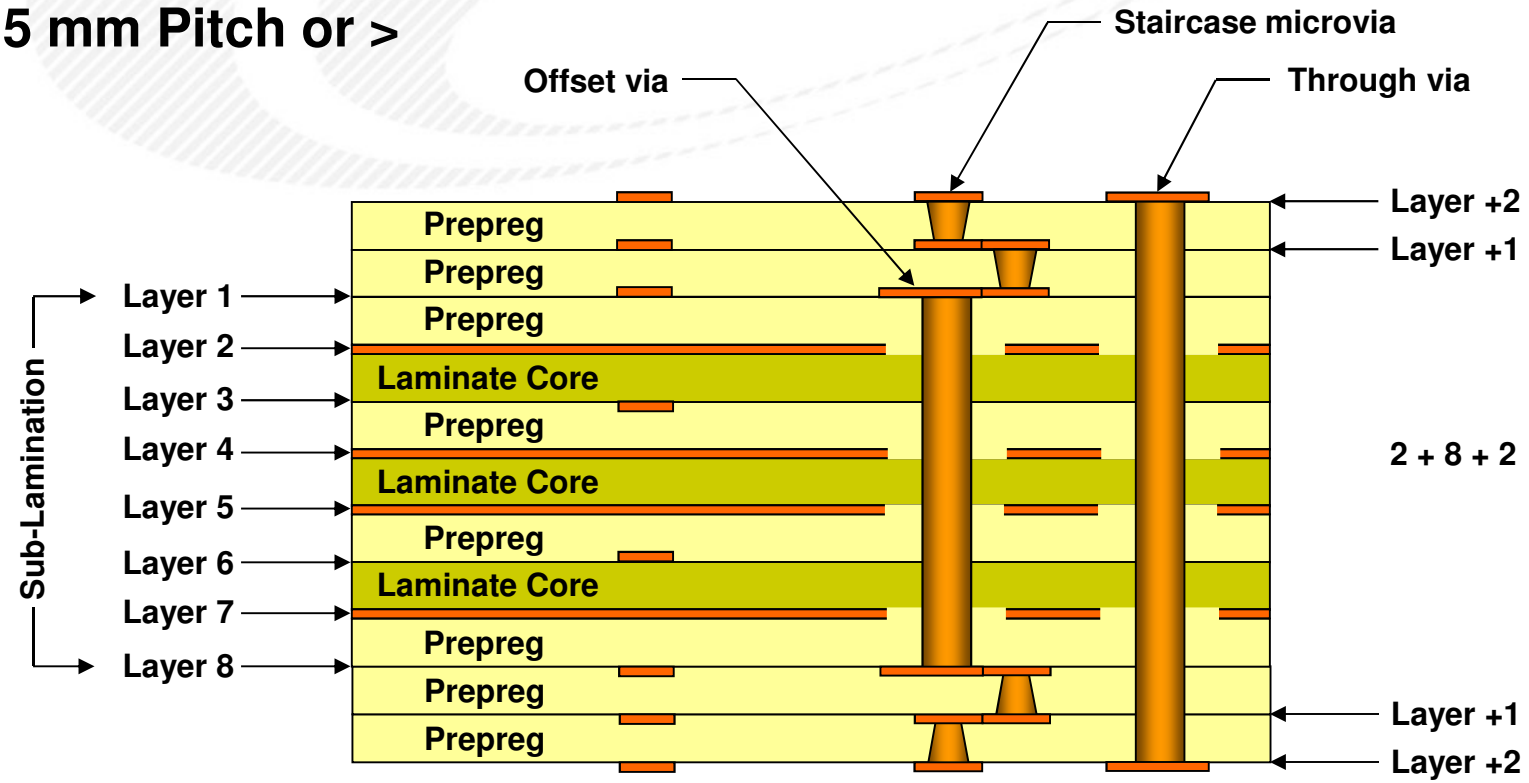
- This approach requires via fill and wrap plating
- CTE issues can be a problem on thick boards



Not Recommended on all designs: Contact engineering

Microvia Sub-Lamination Interface: Offset Via

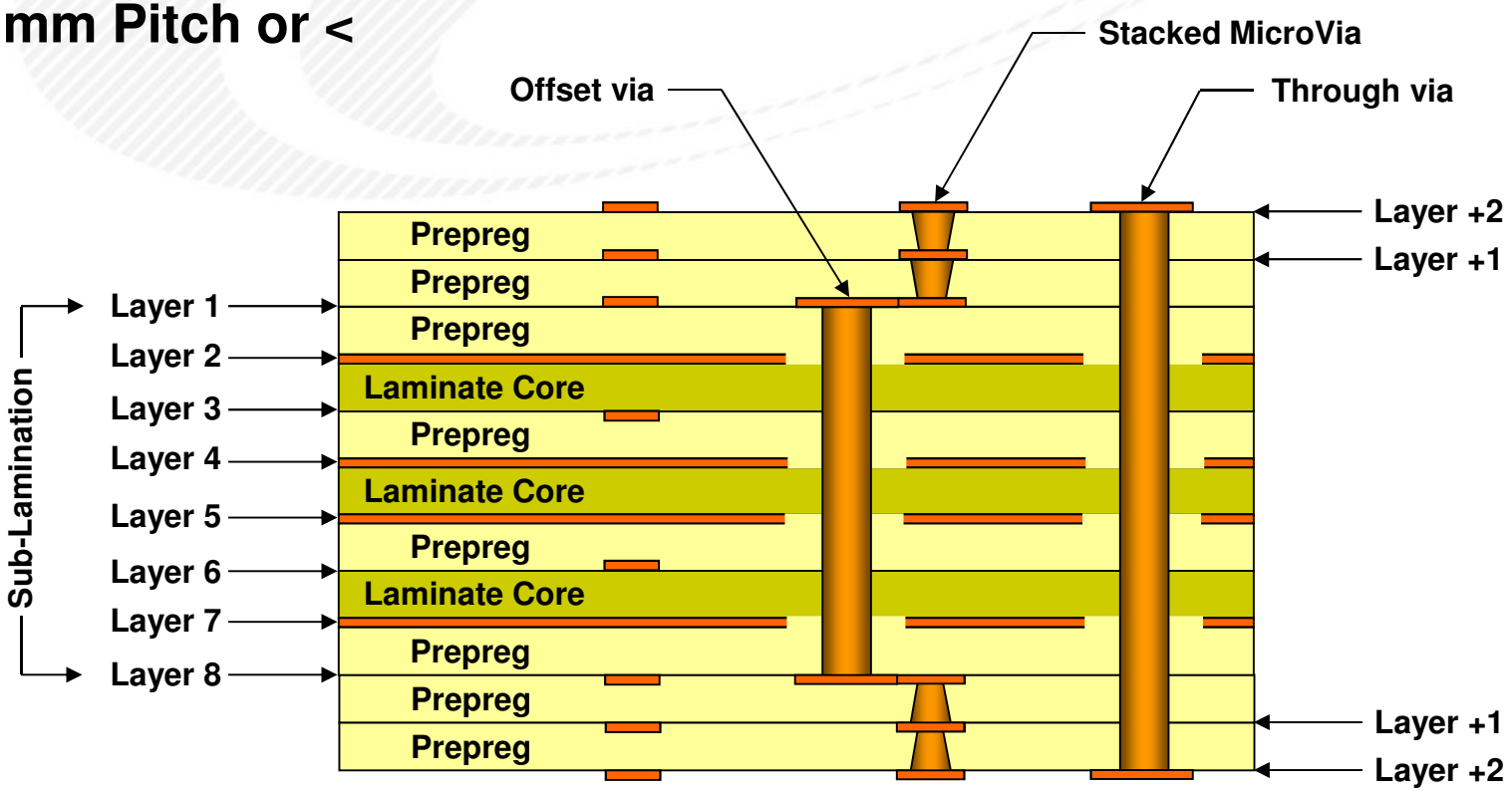
0.5 mm Pitch or >



Preferred Construction

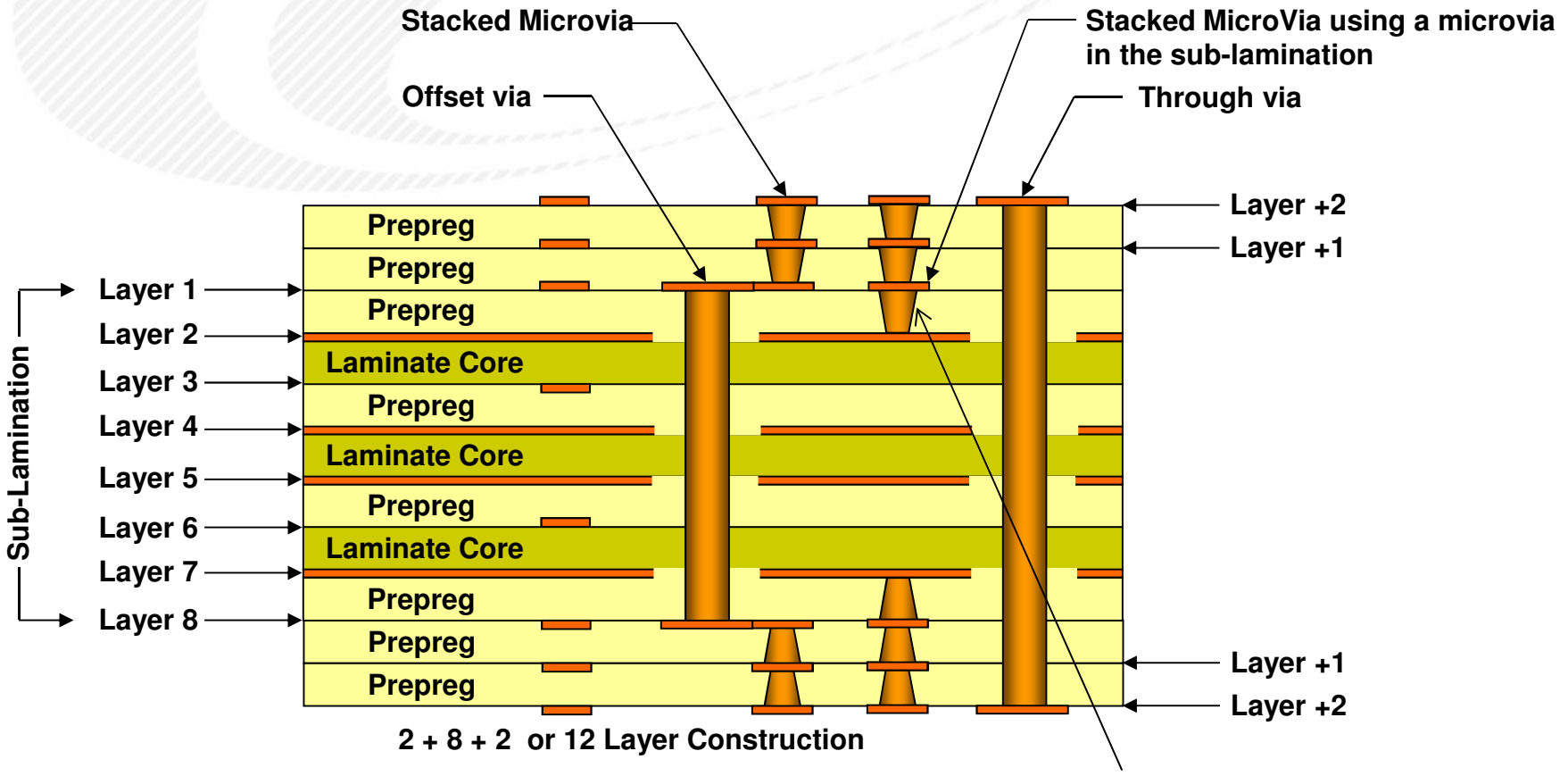
Microvia Sub-Lamination Interface: Offset Via Stacked

0.4 mm Pitch or <



Preferred Construction

Microvia Sub-Lamination Interface: Sub-Lam Microvia



Preferred Construction with additional low cost Microvia to layer 4

Summary

The key to a successful Design is the right combination of Via structures & paths, trace width & space, drill diameter, pad diameter, anti-pad, and aspect ratio. This will maximize routing density, improve electrical characteristics and allows the PCB to be fabricated with high yields for the lowest cost in a timely manner.

Viasystems North America

Thank You!

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